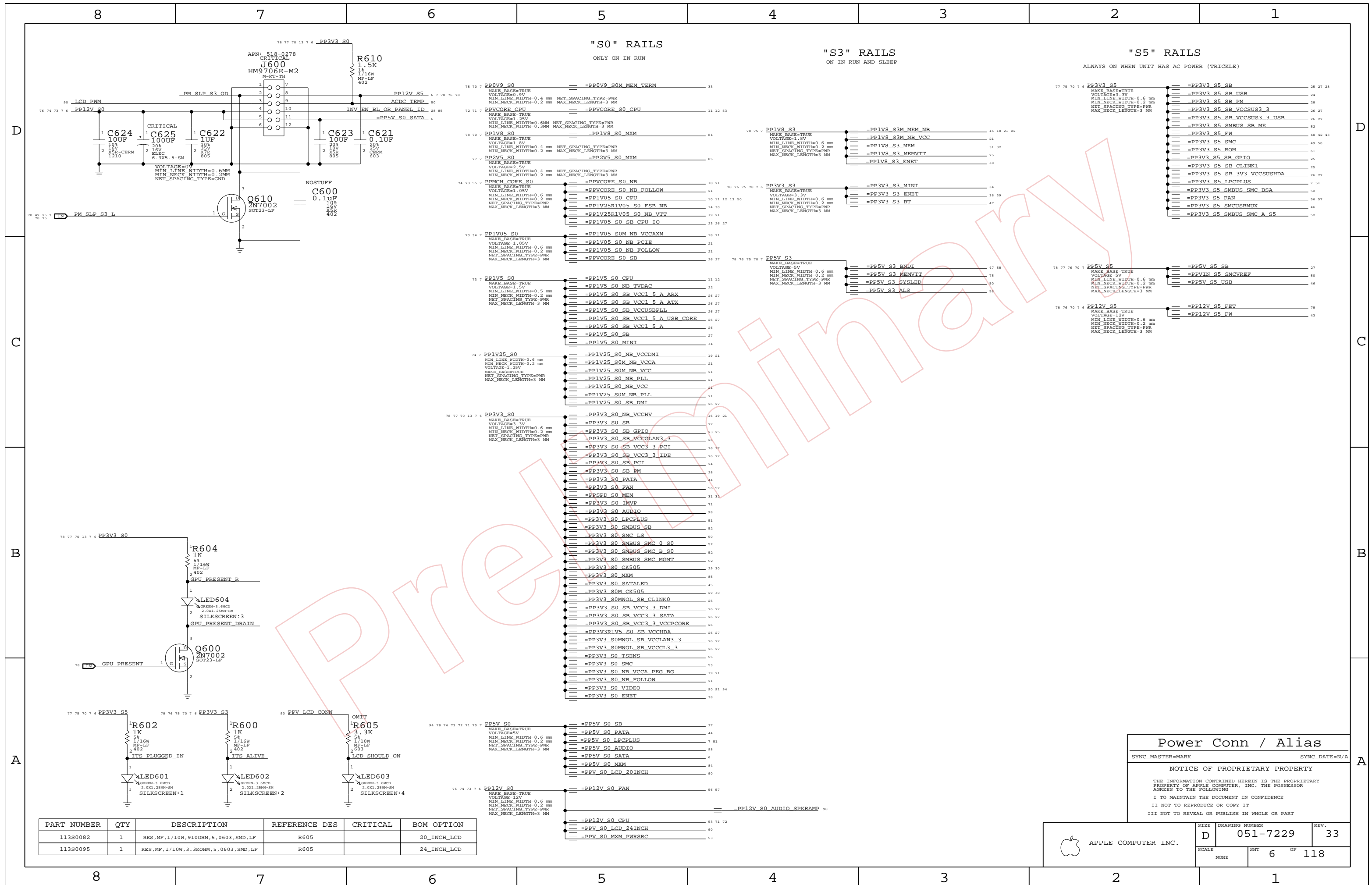
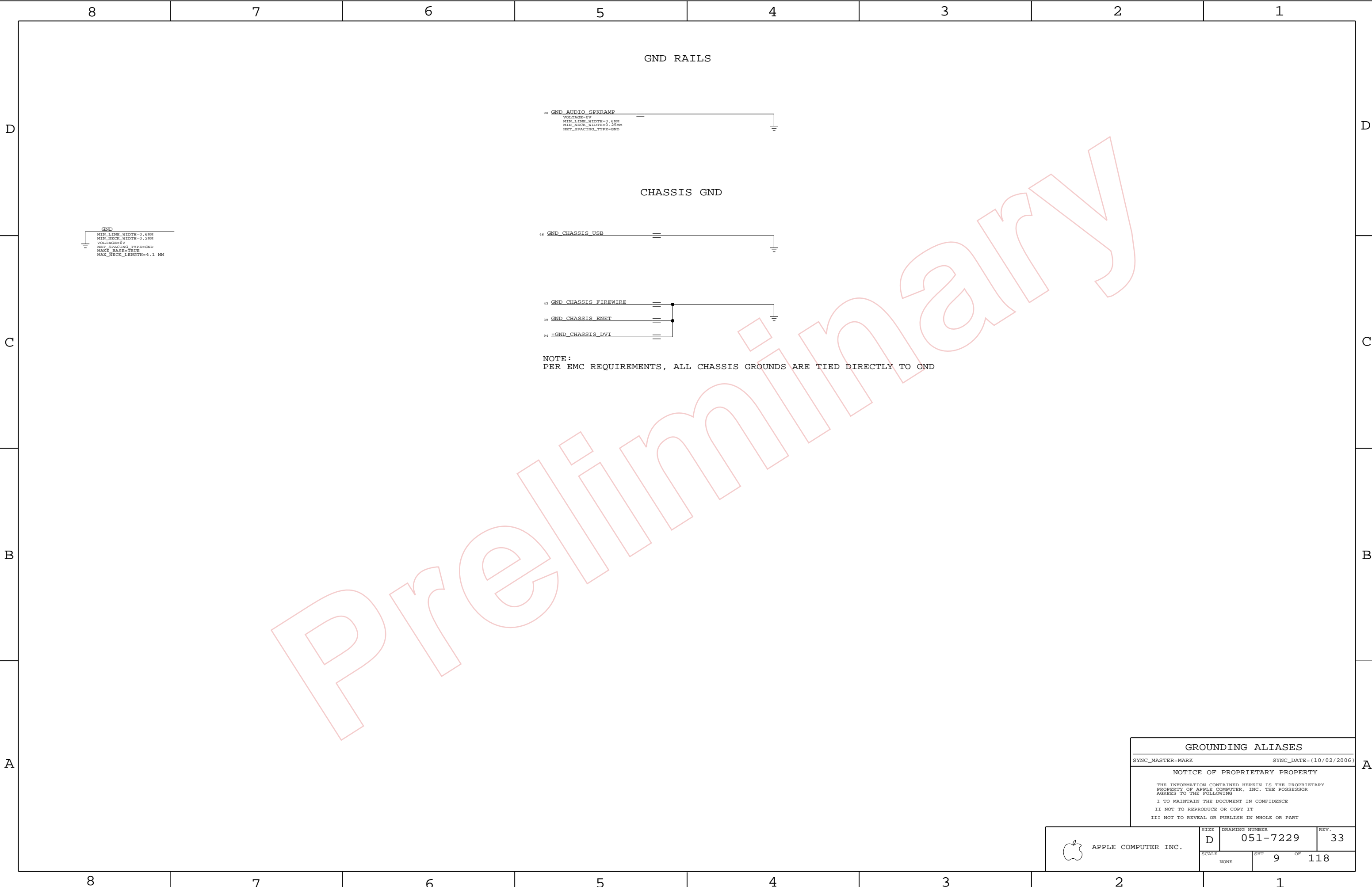


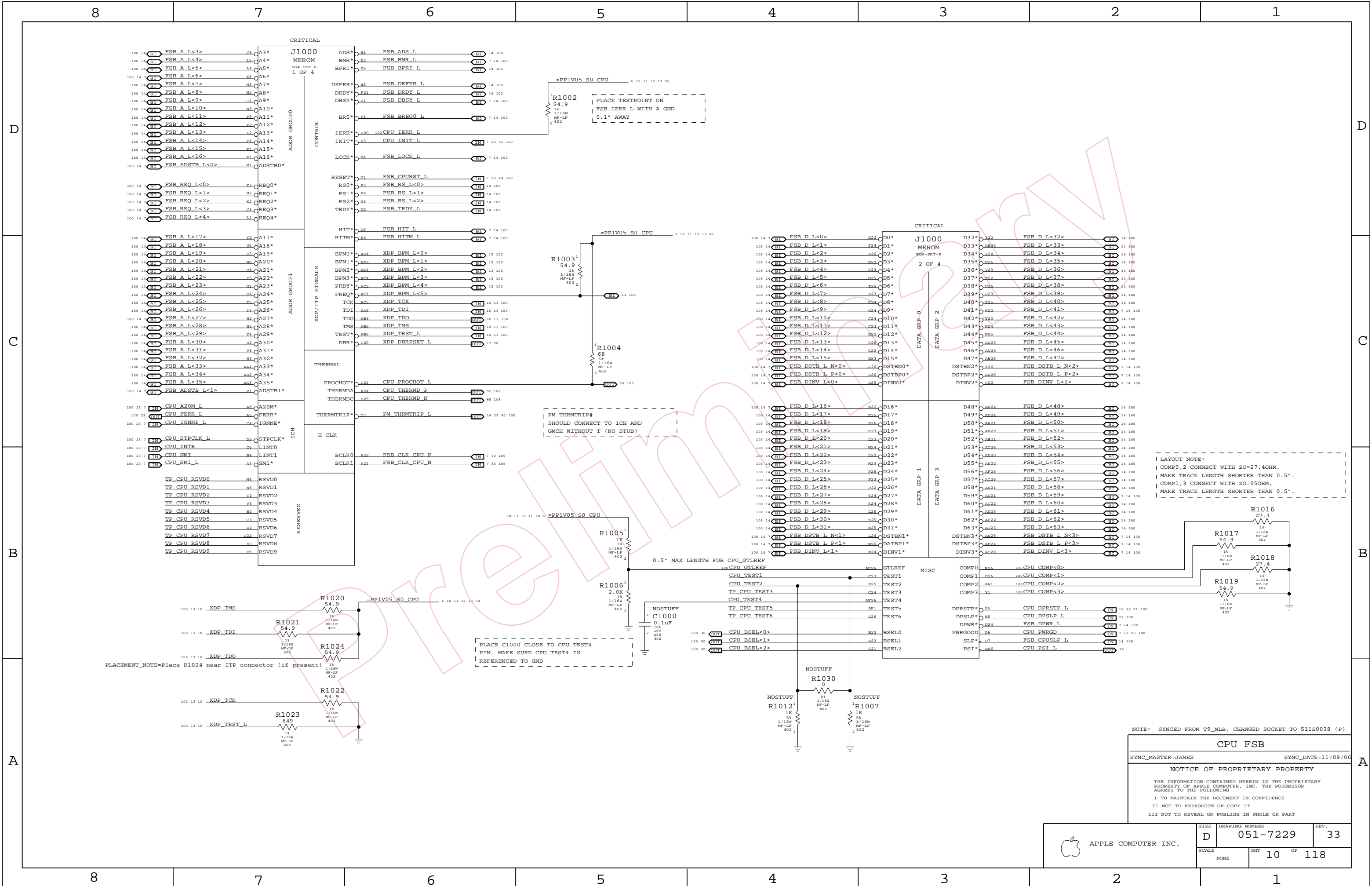
8		7		6		5		4		3		2		1			
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.												REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.												33		503047	ENGINEERING RELEASED	05/09/07	?
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.																	
M78-DVT																	
05/09/2007																	
D	Page (.csa)		Contents		Sync		Date		Page (.csa)		Contents		Sync		Date		
	1	1	Table of Contents		N/A		N/A		79	110	Cross Reference Page						
	2	2	System Block Diagram		DEREK		1/19/2007		80	111	Cross Reference Page						
	3	3	Power Block Diagram		MARK		N/A		81	112	Cross Reference Page						
	4	4	BOM Configuration		JAMES		10/16/06		82	113	Cross Reference Page						
	5	5	Revision History		JAMES		10/16/06		83	114	Cross Reference Page						
	6	6	Power Conn / Alias		MARK		N/A		84	115	Cross Reference Page						
	7	7	Functional / ICT Test		JAMES		10/16/06		85	116	Cross Reference Page						
	8	9	GROUNDING ALIASES		MARK		(10/02/2006)		86	117	Cross Reference Page						
	9	10	CPU FSB		JAMES		11/09/06		87	118	Cross Reference Page						
C	10	11	CPU Power & Ground		JAMES		11/09/06										
	11	12	CPU Decoupling & VID		MARK		10/10/2006										
	12	13	eXtended Debug Port (XDP)		T9_MLB_NOME		11/06/2006										
	13	14	NB CPU Interface		T9_MLB		10/30/2006										
	14	15	NB PEG / Video Interfaces		T9_MLB		10/30/2006										
	15	16	NB Misc Interfaces		T9_MLB		01/21/2007										
	16	17	NB DDR2 Interfaces		T9_MLB		10/30/2006										
	17	18	NB Power 1		T9_MLB		10/30/2006										
	18	19	NB Power 2		T9_MLB		10/30/2006										
	19	20	NB Grounds		T9_MLB		10/30/2006										
B	20	21	NB Standard Decoupling		JAMES		11/03/2006										
	21	22	NB Graphics Decoupling		JAMES		10/16/06										
	22	23	SB Enet, Disk, FSB, LPC		T9_MLB_NOME		03/22/2007										
	23	24	SB PCI, PCIE, DMI, USB		T9_MLB_NOME		03/22/2007										
	24	25	SB Pwr Mgt, GPIO, Clink		T9_MLB_NOME		03/22/2007										
	25	26	SB Power & Ground		T9_MLB_NOME		03/22/2007										
	26	27	SB Decoupling		DAVE_MASTER		N/A										
	27	28	SB Misc		DAVE_MASTER		N/A										
	28	29	Clock (CK505)		JAMES		11/27/2006										
	29	30	Clock Termination		JAMES		10/18/2006										
A	30	31	DDR2 SO-DIMM Connector A		JAMES		10/17/06										
	31	32	DDR2 SO-DIMM Connector B		JAMES		10/17/06										
	32	33	Memory Active Termination		JAMES		12/04/2006										
	33	34	PCI-E MiniCard Connector		DOUG		10/30/2006										
	34	37	Ethernet (Yukon)		DOUG		11/08/2006										
	35	38	YUKON/ULTRA SUPPORT		DOUG		(10/02/2006)										
	36	39	ETHERNET CONNECTOR		DOUG		11/06/2006										
	37	40	FW: 1394B CONTROLLER		M78_MLB		12/15/2006										
	38	42	FW: 1394B MISC		DOUG		10/10/2006										
	39	43	FIREWIRE CONNECTORS		DOUG		10/10/2006										
<div>DRAWING</div> <div>TITLE=M78</div> <div>ABBREV=DRAWING</div> <div>LAST_MODIFIED=Wed May 9 10:26:54 2007</div>																	
8		7		6		5		4		3		2		1			

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX : _____		NOTICE OF PROPRIETARY PROPERTY		THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE I: NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
X.XX : _____		DRAFTER			

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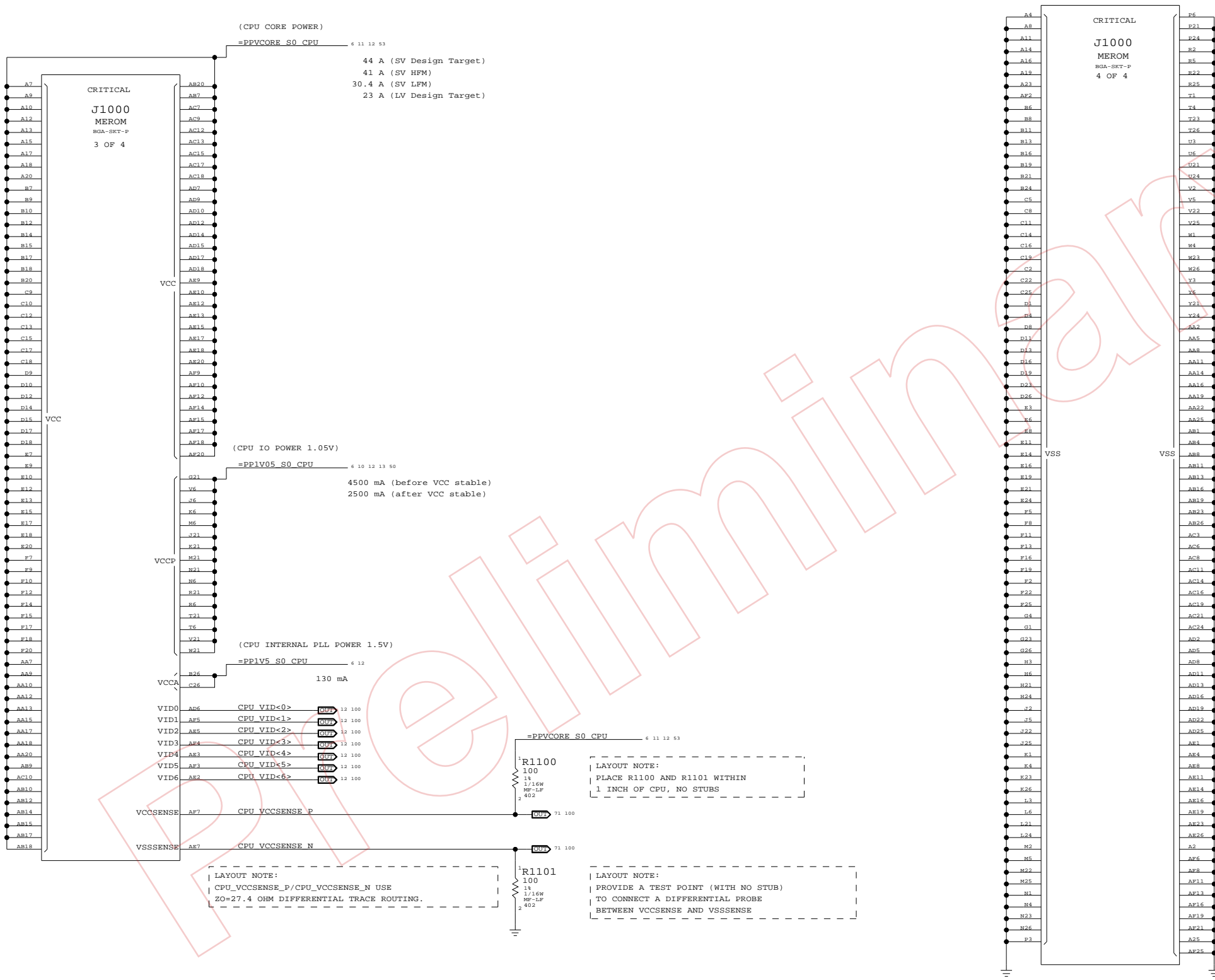
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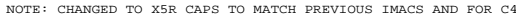


NOTE: SYNCED FROM T9_MLB, CHANGED SOCKET TO 511S0038 (P)

CPU Power & Ground	
SYNC_MASTER=JAMES	SYNC_DATE=11/09/06
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	D	051-7229	33
SCALE		SHT	OF
NONE		11	118

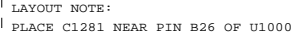
6X 220UF. 32X 22UF 0805



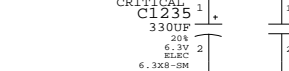
~~Resistors to allow for override of CPU VID
Will probably be removed before production~~




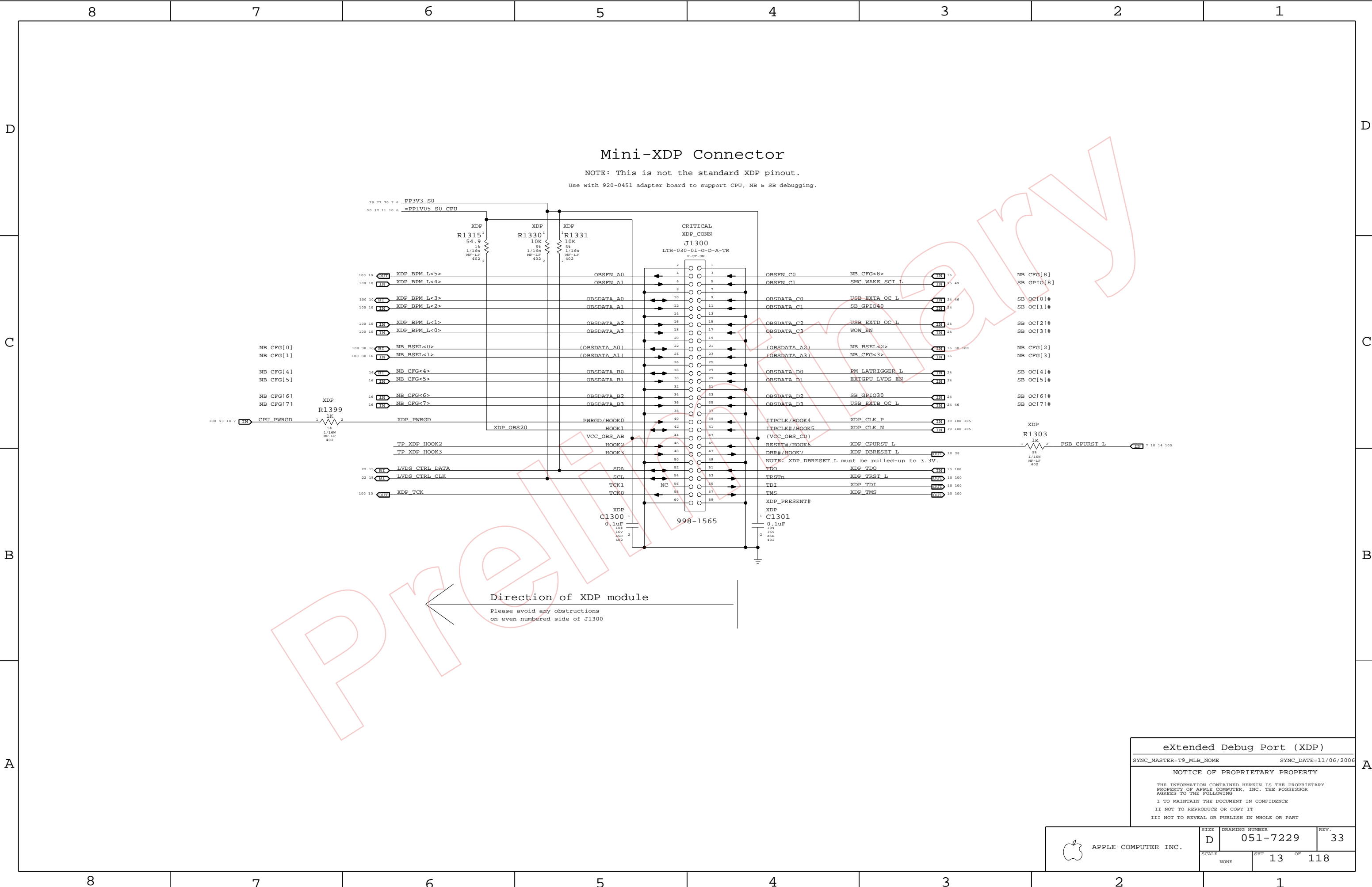
VCCA (CPU AVdd) DECOUPLING



VCCP (CPU I/O) DECOUPLING



 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7229	33
	SCALE	SHT	OF
	NONE	12	118



eXtended Debug Port (XDP)

SYNC_MASTER=T9_MLB_NAME SYNC_DATE=11/06/2006

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SCALE		SHT	OF
NONE		13	118

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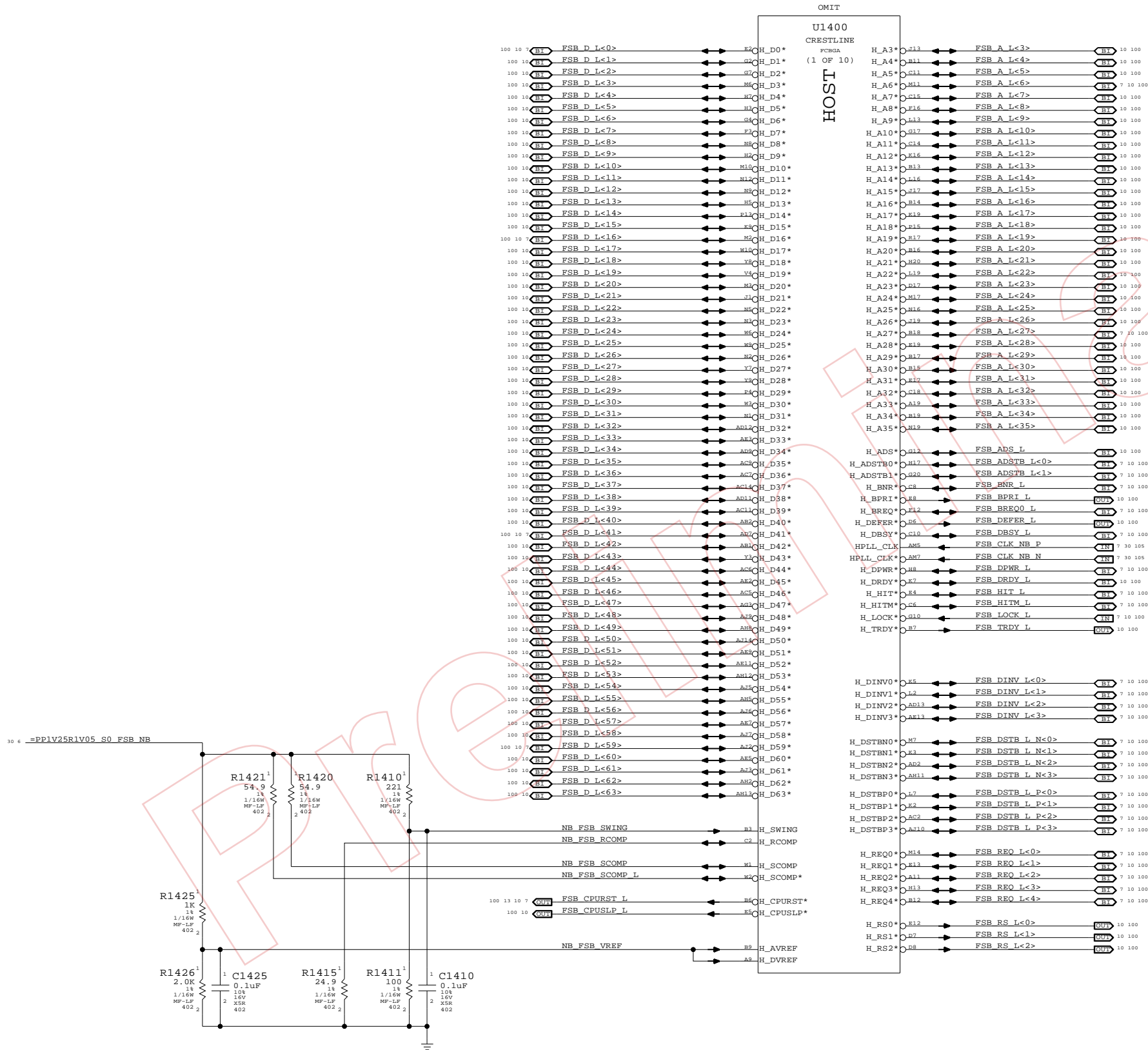
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NB CPU Interface

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

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	D	051-7229	33
SCALE		SHT	OF
NONE		14	118

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D

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A

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTIN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

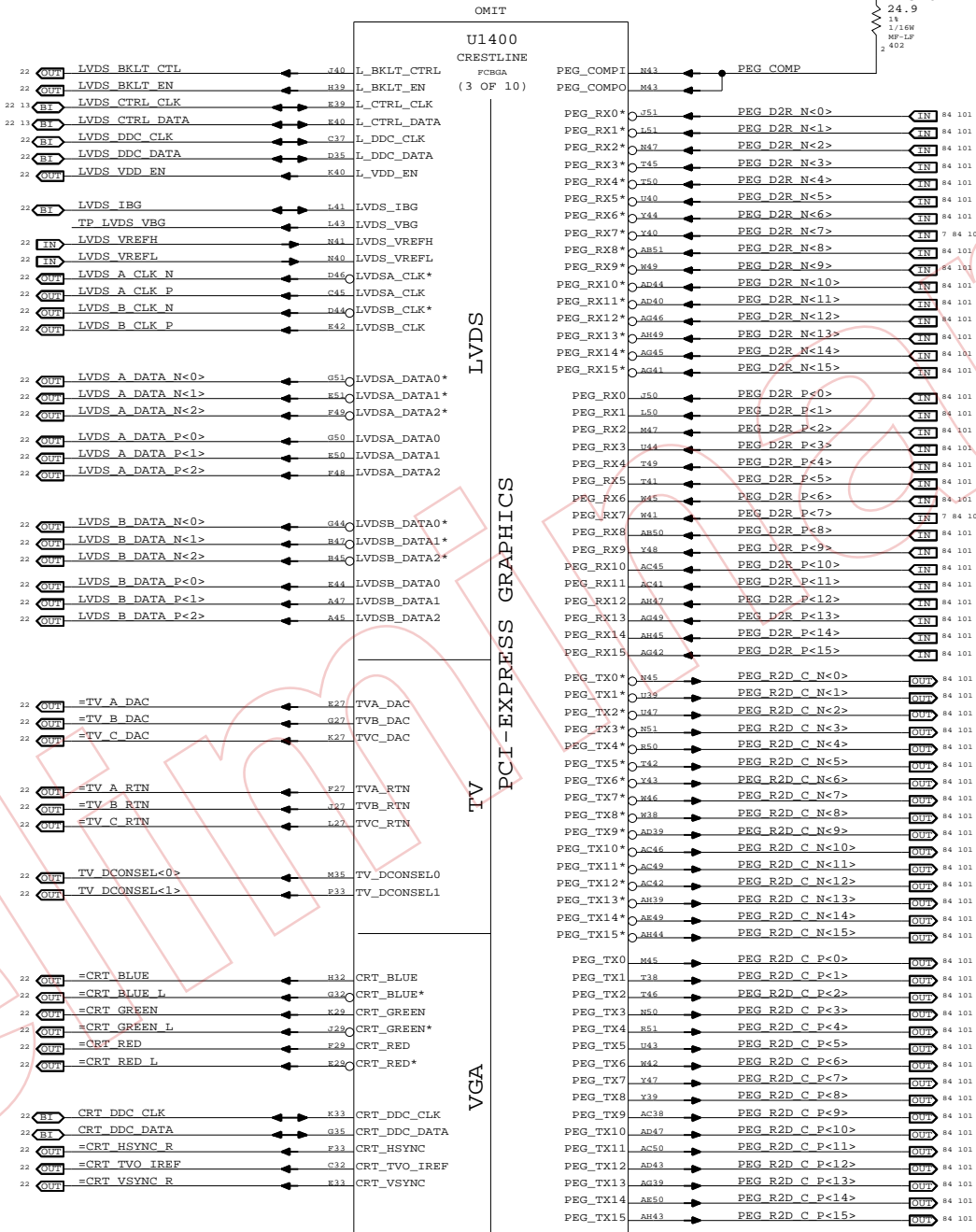
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTIN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLL and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



NB PEG / Video Interfaces

SYNC_MASTER=TS_MLB

SYNC_DATE=10/30/2006

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DRAWING NUMBER

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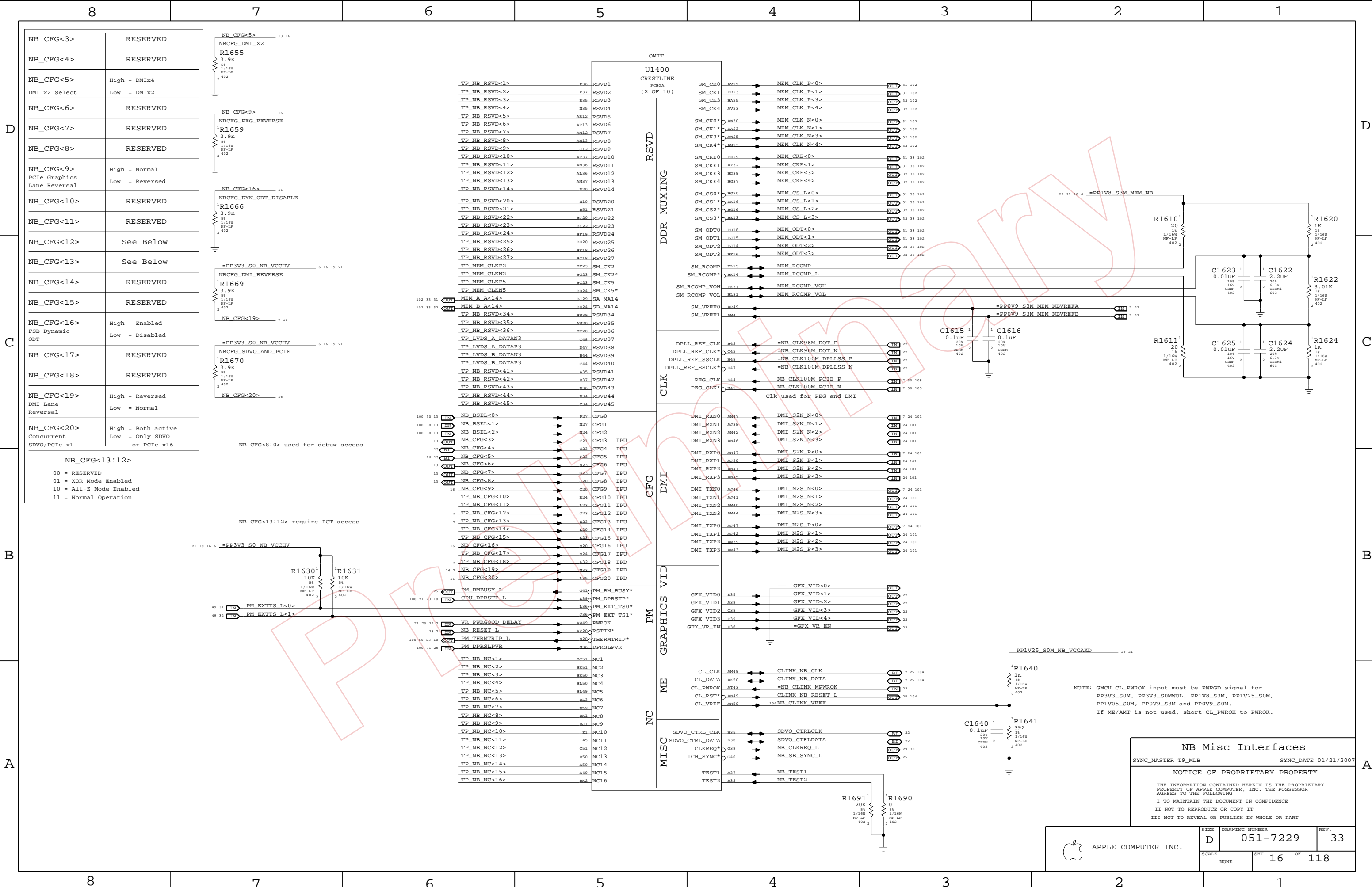
NONE

SHT

15

OF

118



NB Misc Interfaces

SYNC_MASTER=TS_MLB SYNC_DATE=01/21/2007

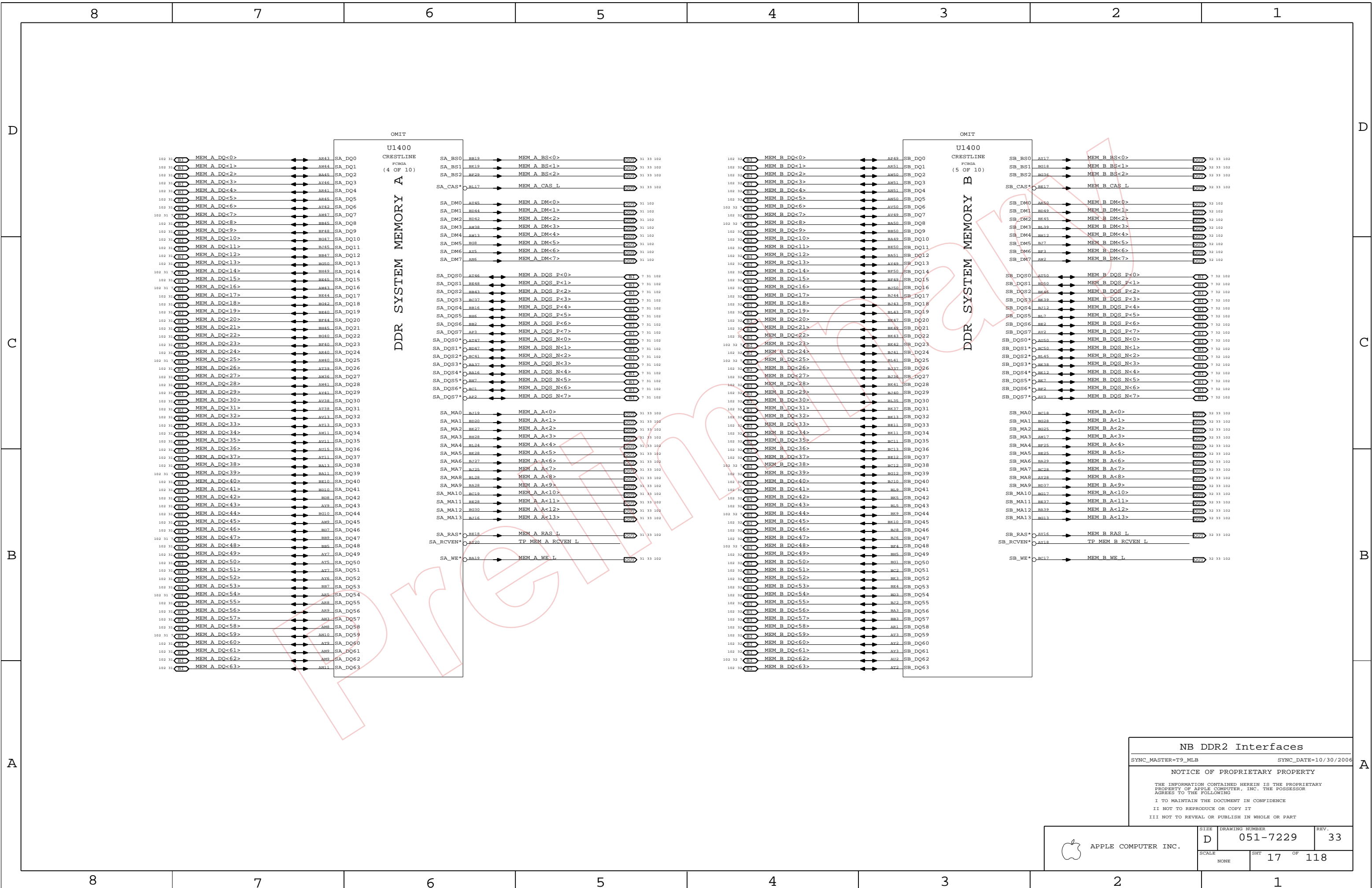
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NB DDR2 Interfaces

SYNC_MASTER=TS_MLB SYNC_DATE=10/30/2006

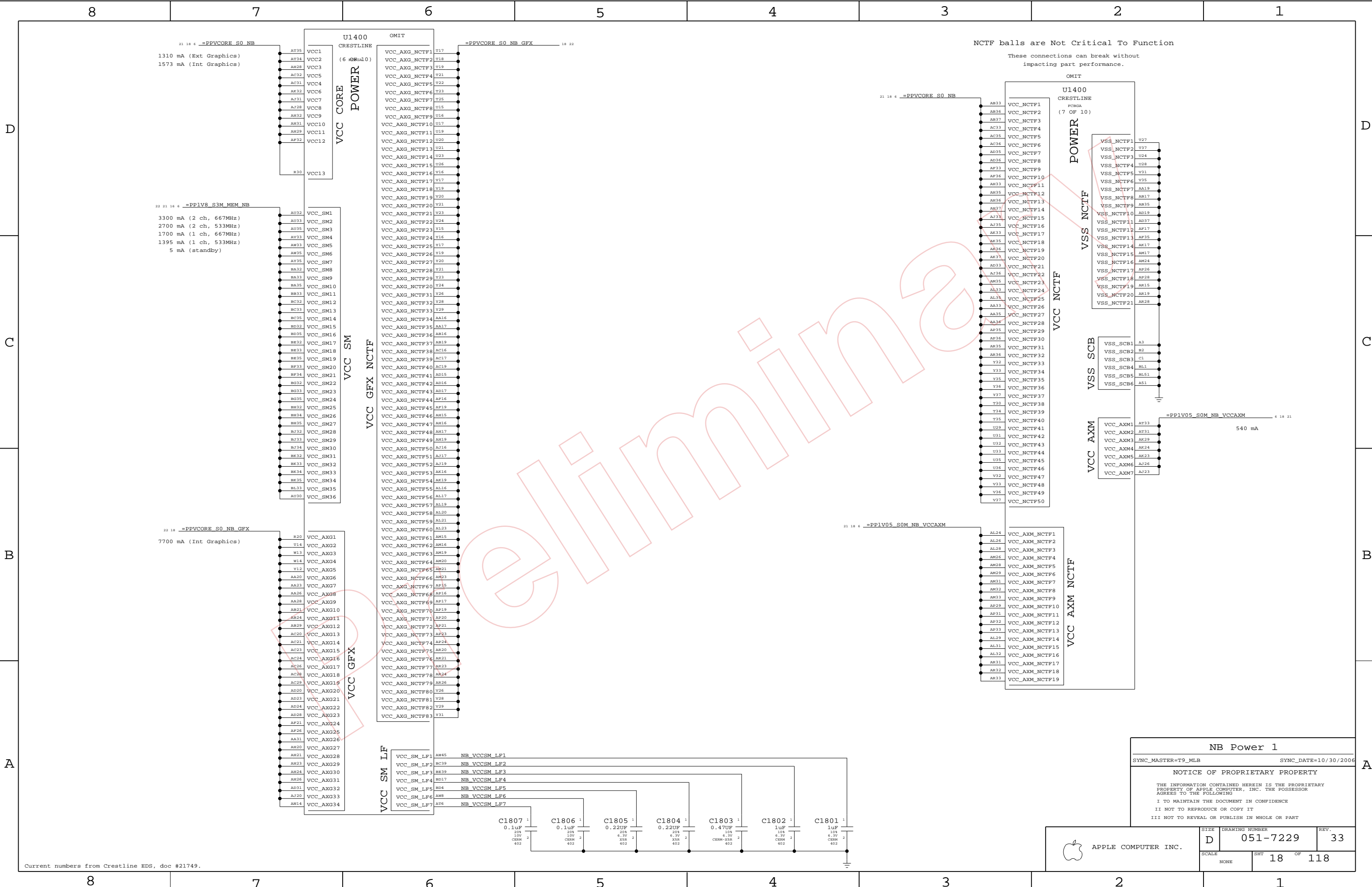
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Current numbers from Crestline EDS, doc #21749.

NB Power 1

SYNC_MASTER=T9_MLB

SYNC_DATE=10/30/2006

NOTICE OF PROPRIETARY PROPERTY

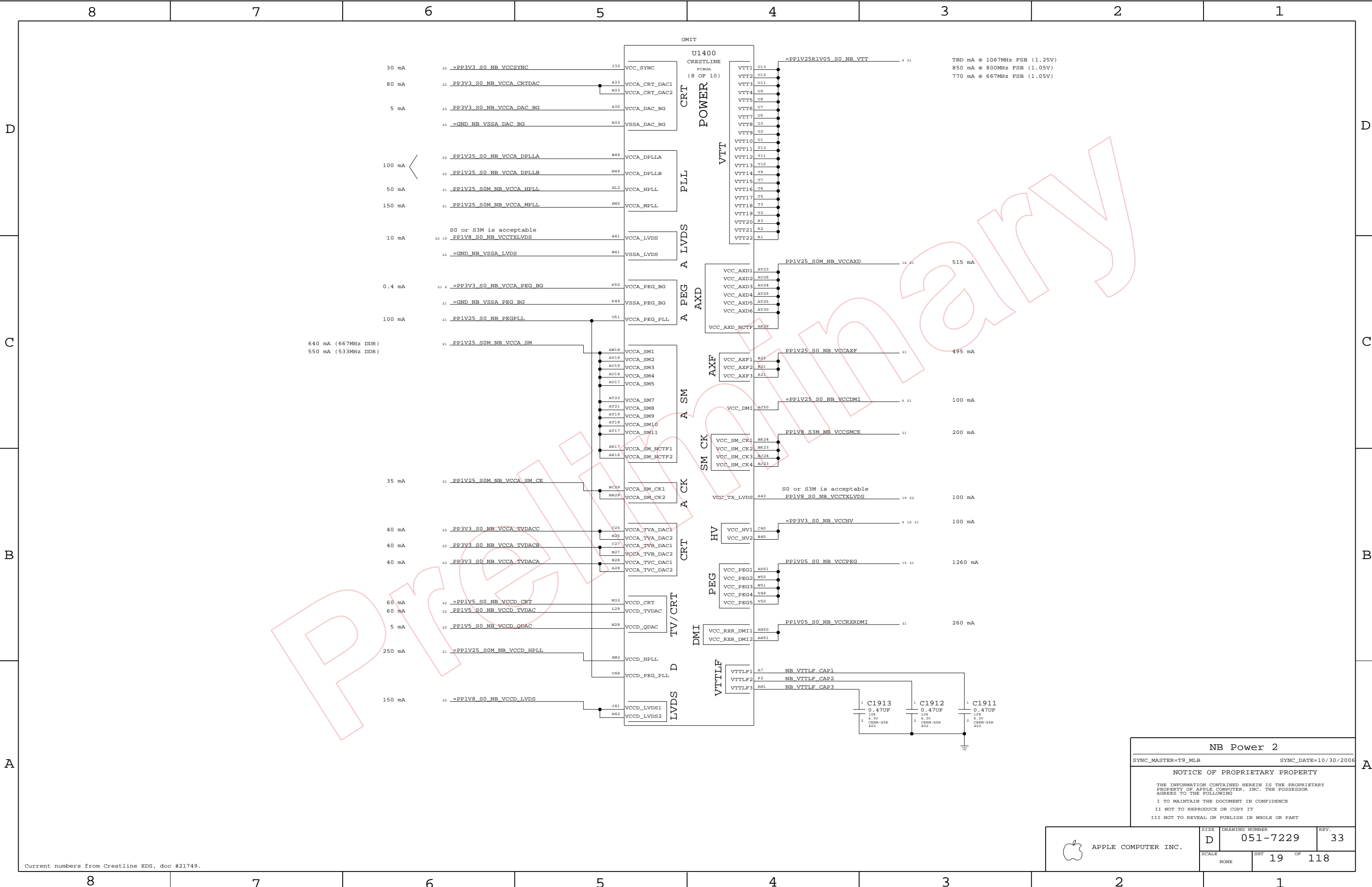
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SCALE		SHT	OF
NONE		18	118



NB Power 2

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

NOTICE OF PROPRIETARY PROPERTY

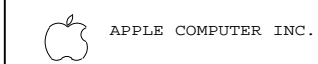
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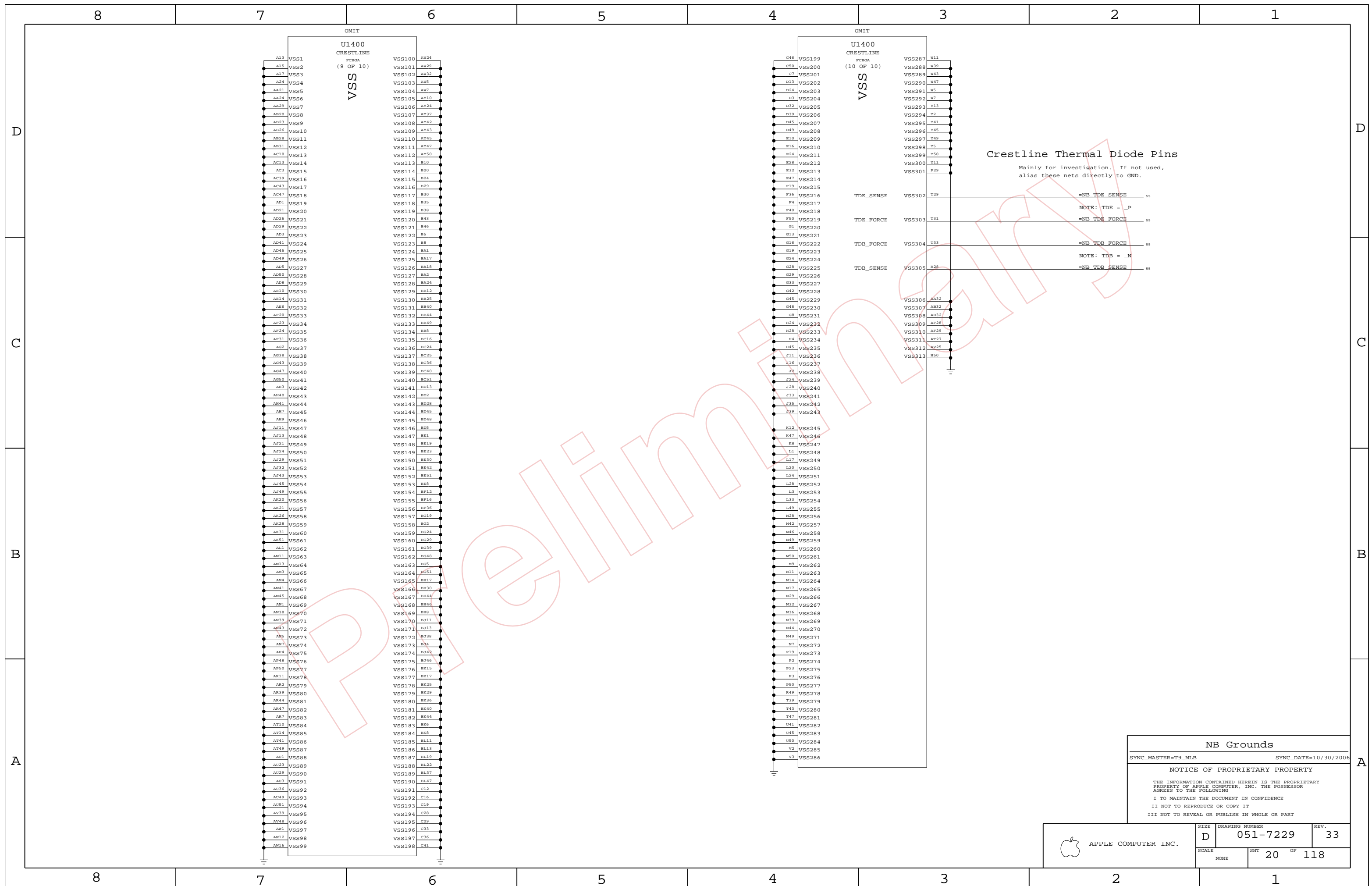
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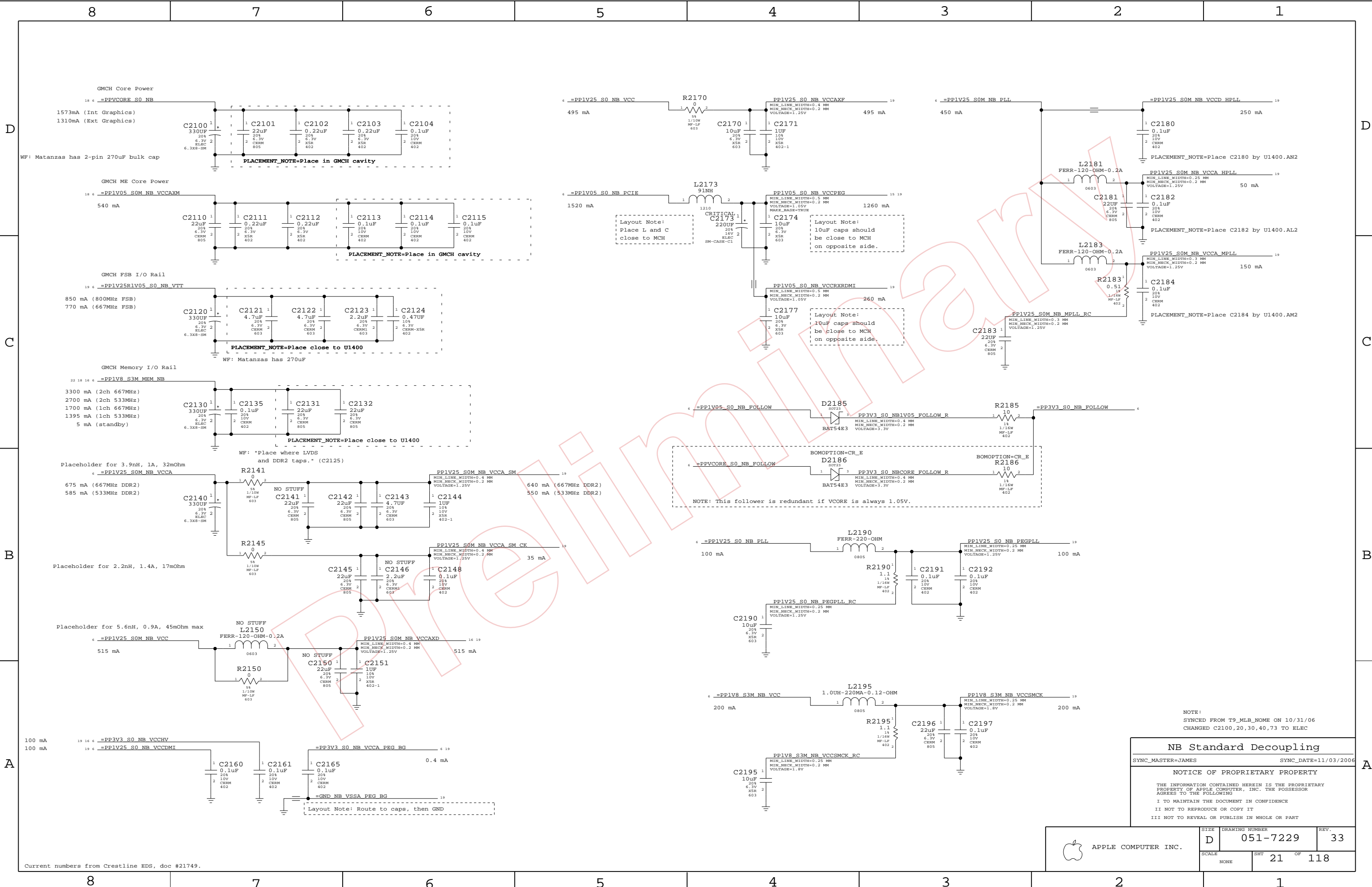
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART


SIZE	DRAWING NUMBER		REV.
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SCALE		SHT	OF
NONE		19	118



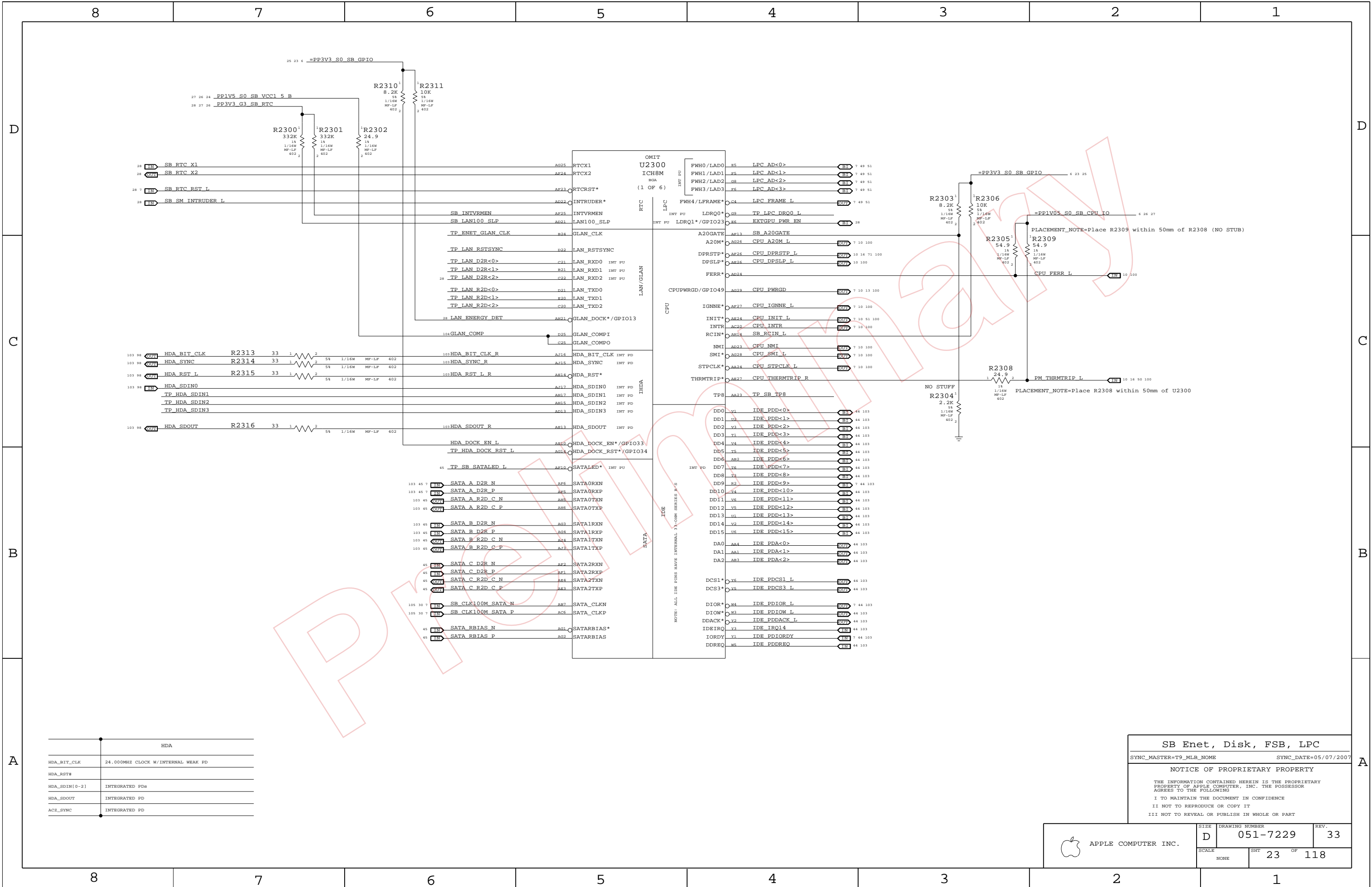


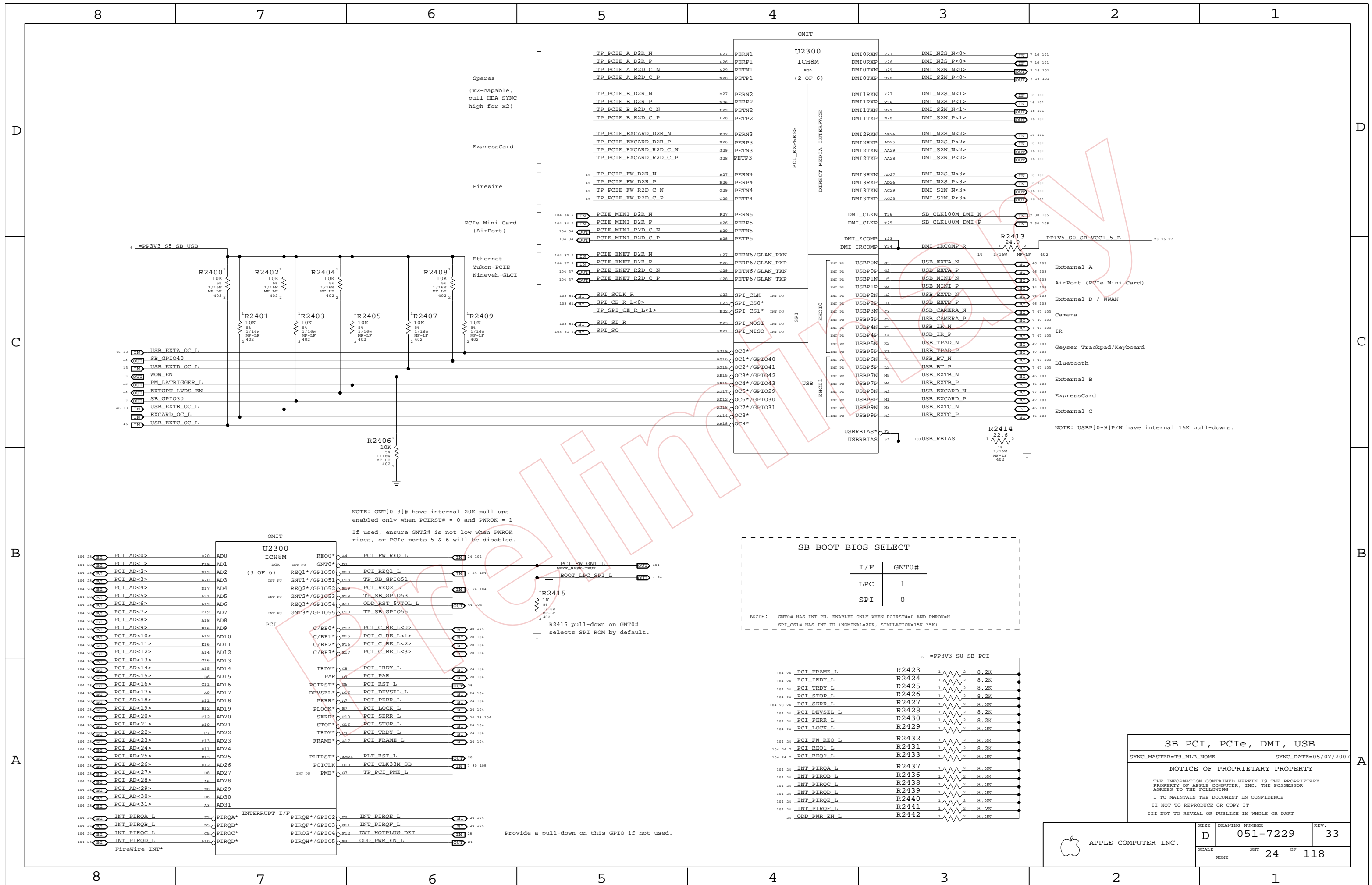


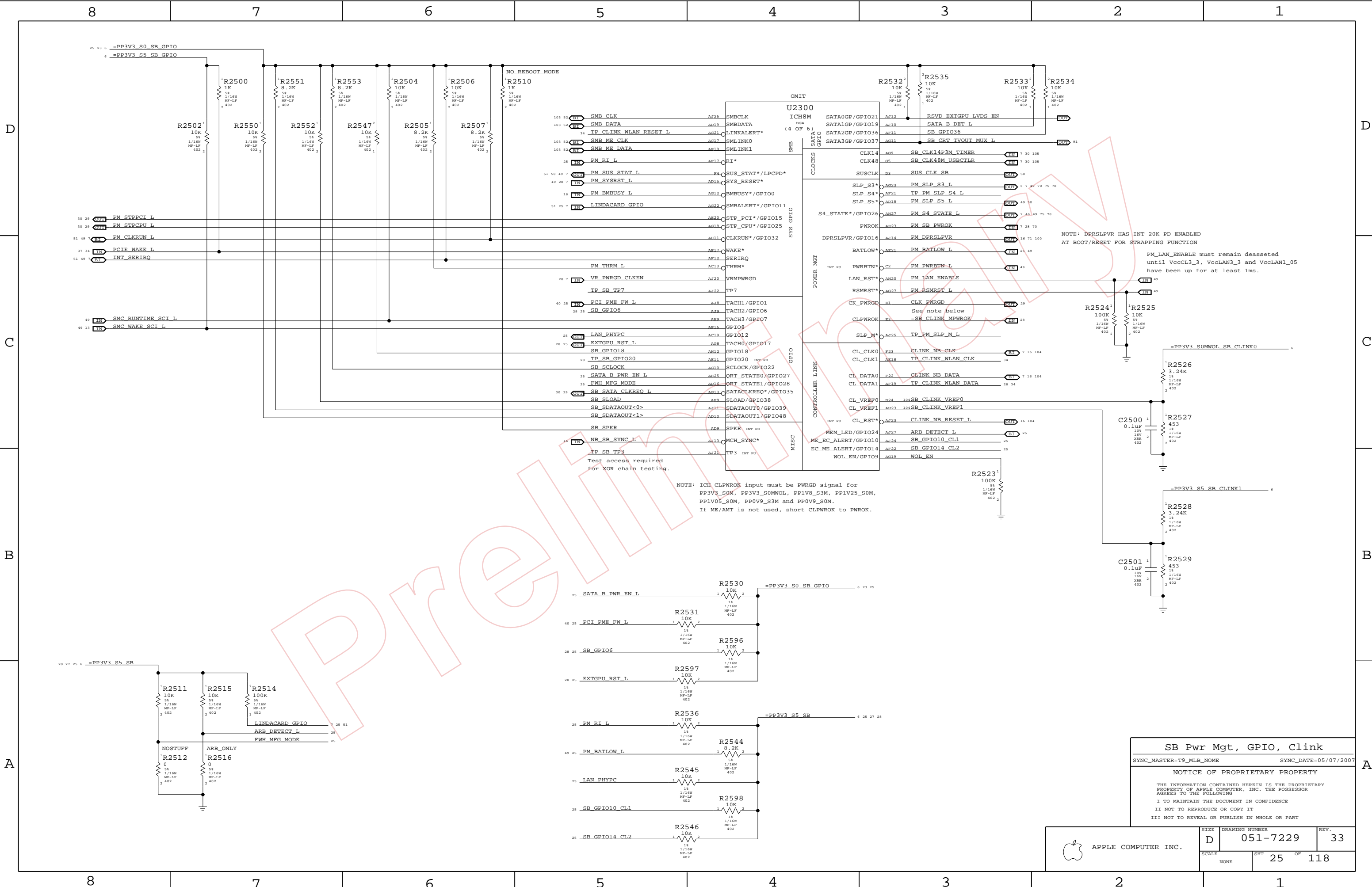
NB Standard Decoupling	
SYNC_MASTER=JAMES	SYNC_DATE=11/03/2006
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	D	051-7229	33
SCALE	SHT	21	OF 118
NONE			

Current numbers from Crestline EDS, doc #21749.







SB Pwr Mgt, GPIO, Clink

SYNC_MASTER=TS_MLB_NOME SYNC_DATE=05/07/2007

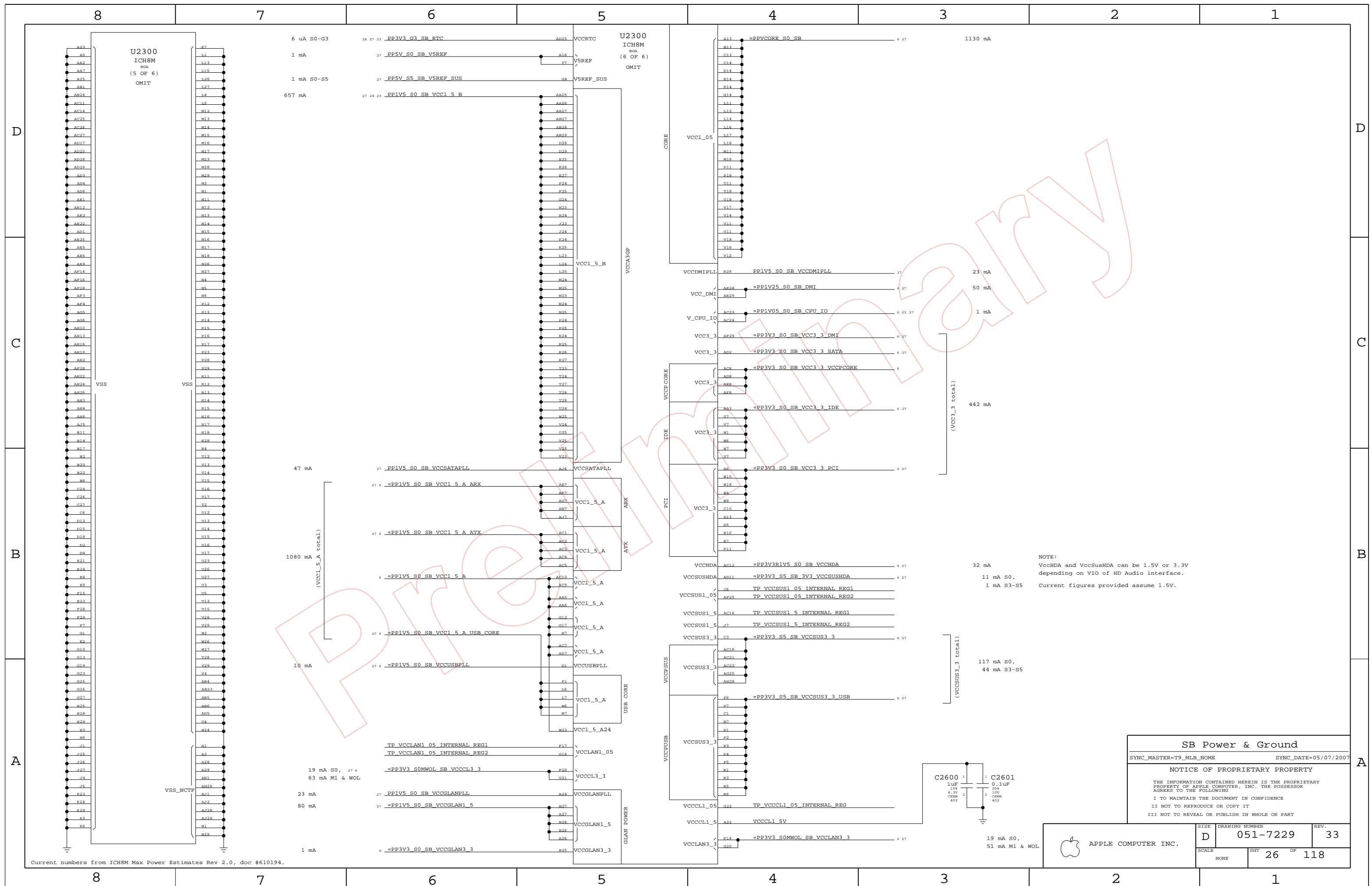
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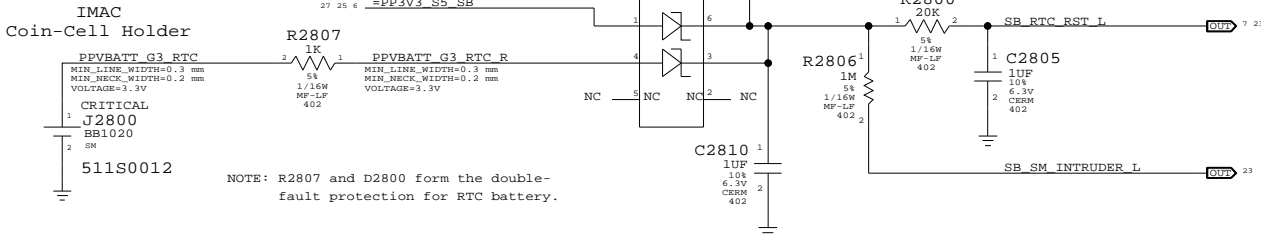
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II NOT TO REPRODUCE OR COPY IT

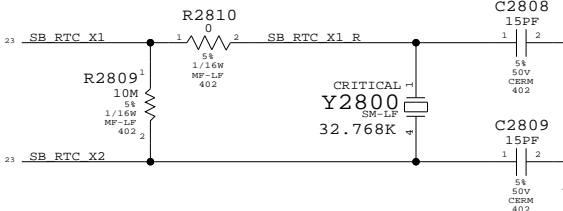
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



RTC Power Sources



SB RTC Crystal



UNUSED PCI BUS

```

1004 24  PCI AD<0> == MAKE_BASE=TRUE TP PCI AD 0
1004 24  PCI AD<1> == MAKE_BASE=TRUE TP PCI AD 1
1004 24  PCI AD<2> == MAKE_BASE=TRUE TP PCI AD 2
1004 24  PCI AD<3> == MAKE_BASE=TRUE TP PCI AD 3
1004 24  PCI AD<4> == MAKE_BASE=TRUE TP PCI AD 4 NO_TEST=TRUE
1004 24  PCI AD<5> == MAKE_BASE=TRUE TP PCI AD 5
1004 24  PCI AD<6> == MAKE_BASE=TRUE TP PCI AD 6
1004 24  PCI AD<7> == MAKE_BASE=TRUE TP PCI AD 7
1004 24  PCI AD<8> == MAKE_BASE=TRUE TP PCI AD 8
1004 24  PCI AD<9> == MAKE_BASE=TRUE TP PCI AD 9
1004 24  PCI AD<10> == MAKE_BASE=TRUE TP PCI AD 10
1004 24  PCI AD<11> == MAKE_BASE=TRUE TP PCI AD 11
1004 24  PCI AD<12> == MAKE_BASE=TRUE TP PCI AD 12
1004 24  PCI AD<13> == MAKE_BASE=TRUE TP PCI AD 13
1004 24  PCI AD<14> == MAKE_BASE=TRUE TP PCI AD 14
1004 24  PCI AD<15> == MAKE_BASE=TRUE TP PCI AD 15
1004 24  PCI AD<16> == MAKE_BASE=TRUE TP PCI AD 16
1004 24  PCI AD<17> == MAKE_BASE=TRUE TP PCI AD 17
1004 24  PCI AD<18> == MAKE_BASE=TRUE TP PCI AD 18
1004 24  PCI AD<19> == MAKE_BASE=TRUE TP PCI AD 19
1004 24  PCI AD<20> == MAKE_BASE=TRUE TP PCI AD 20
1004 24  PCI AD<21> == MAKE_BASE=TRUE TP PCI AD 21
1004 24  PCI AD<22> == MAKE_BASE=TRUE TP PCI AD 22
1004 24  PCI AD<23> == MAKE_BASE=TRUE TP PCI AD 23
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1004 24  PCI AD<26> == MAKE_BASE=TRUE TP PCI AD 26
1004 24  PCI AD<27> == MAKE_BASE=TRUE TP PCI AD 27
1004 24  PCI AD<28> == MAKE_BASE=TRUE TP PCI AD 28
1004 24  PCI AD<29> == MAKE_BASE=TRUE TP PCI AD 29
1004 24  PCI AD<30> == MAKE_BASE=TRUE TP PCI AD 30
1004 24  PCI AD<31> == MAKE_BASE=TRUE TP PCI AD 31

1004 24  PCI C BE L<0> == MAKE_BASE=TRUE TP PCI C BE L 0
1004 24  PCI C BE L<1> == MAKE_BASE=TRUE TP PCI C BE L 1
1004 24  PCI C BE L<2> == MAKE_BASE=TRUE TP PCI C BE L 2
1004 24  PCI C BE L<3> == MAKE_BASE=TRUE TP PCI C BE L 3
1004 24  PCI RST L == MAKE_BASE=TRUE TP PCI RST L
1004 24  PCI PAR == MAKE_BASE=TRUE TP PCI PAR

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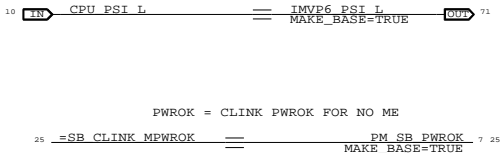
NO TEST DUE TO ROUTING

```

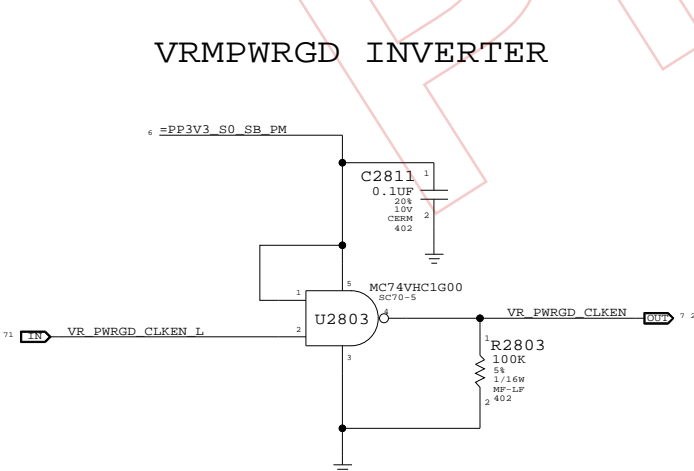
23  IN TP LAN D2R<2> NO_TEST=TRU
34 25 IN TP CLINK WLAN DATA NO_TEST=TRU
104 24 IN PCI SERR L NO_TEST=TRU

```

CPU VCORE FORCEPSI UNUSED

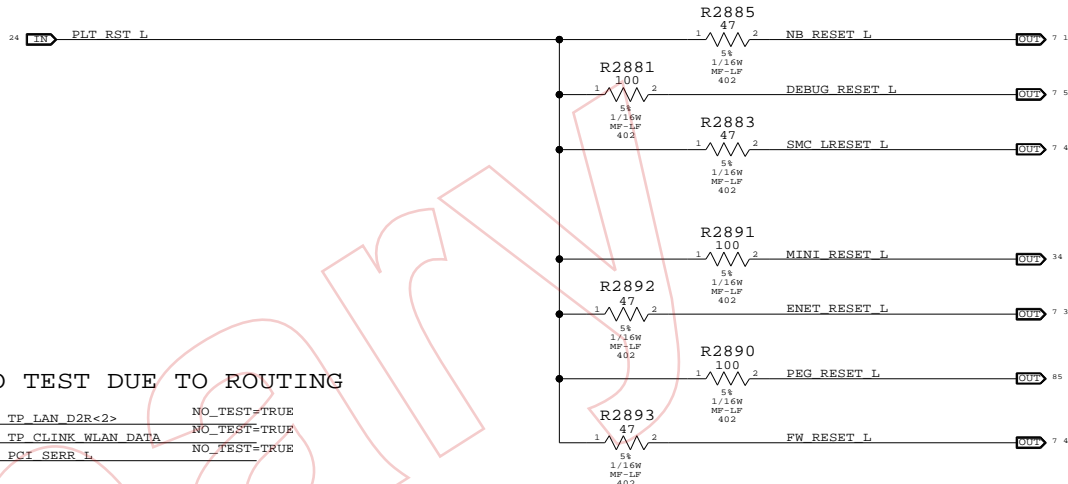


~~VRMPWRGD INVERTER~~

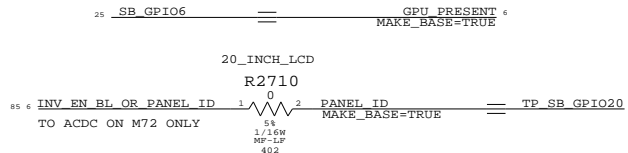


Platform Reset Connection

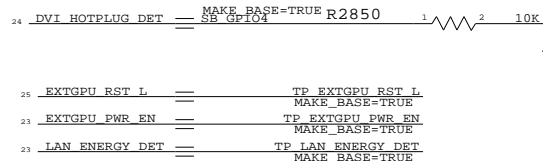
Unbuffere



RE-PURPOSED GPIO



UNUSED GPIO



SB Misc

SYNC_MASTER=DAVE_MASTER	SYNC_DATE=N
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APPLE COMPUTER IN

SIZE	DRAWING NUMBER	REVISION
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D	051-7229	3
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DATE	28	11
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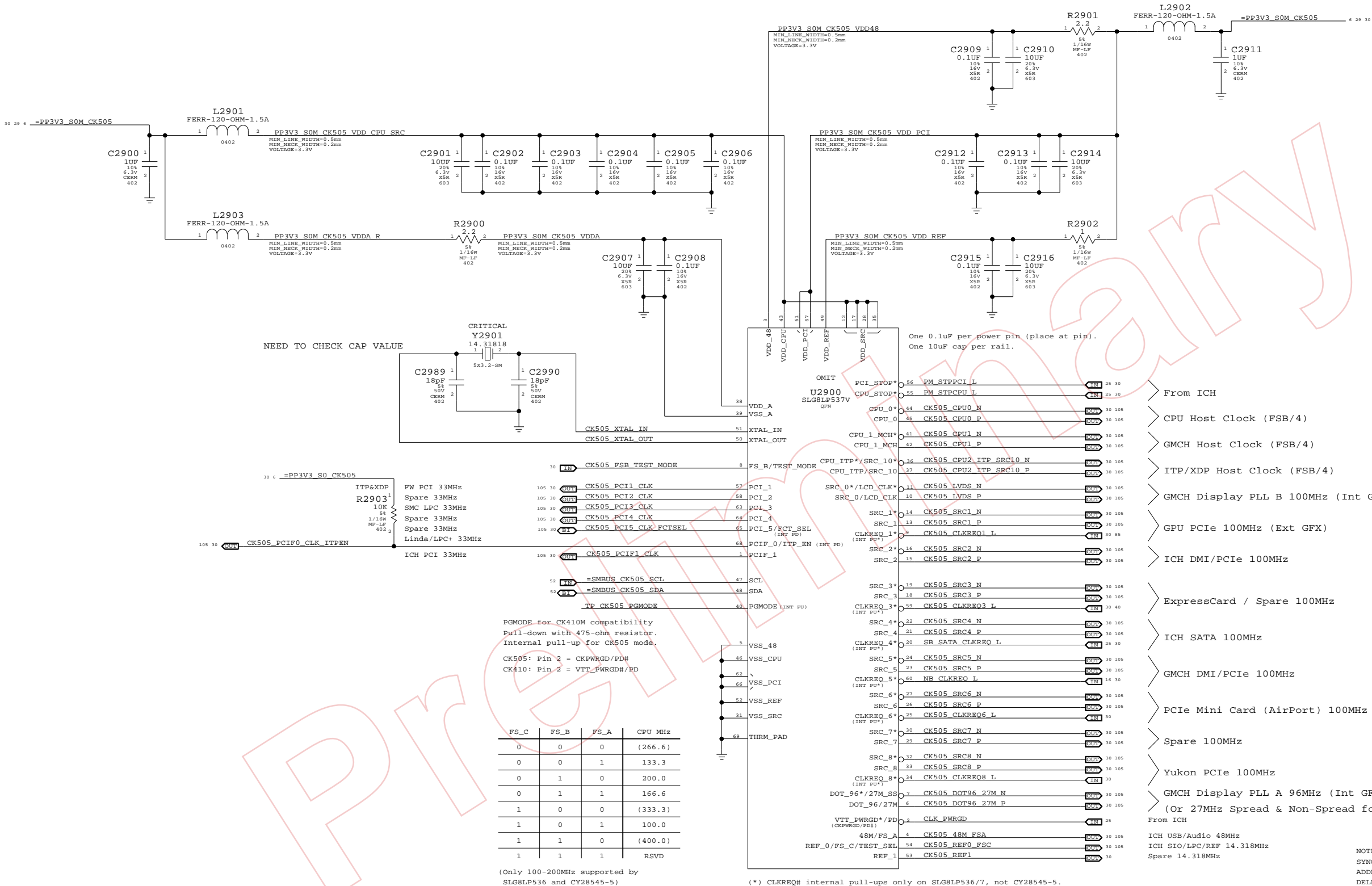
5

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3

2

1



FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-
1	27M	27M w/SS	SRC_0+	SRC_0-

(For Internal Graphics)
(For External Graphics)

Clock (CK505)

SYNC_MASTER=JAMES SYNC_DATE=11/27/2006

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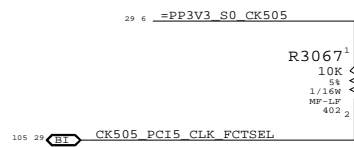
SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE	SHT	OF
NONE	29	118

CLK Termination

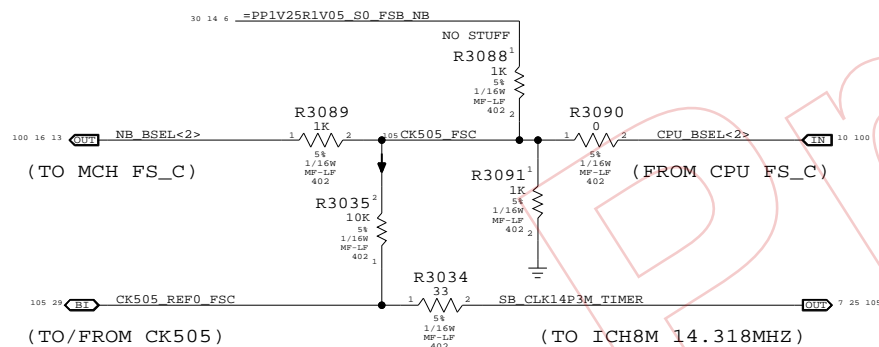
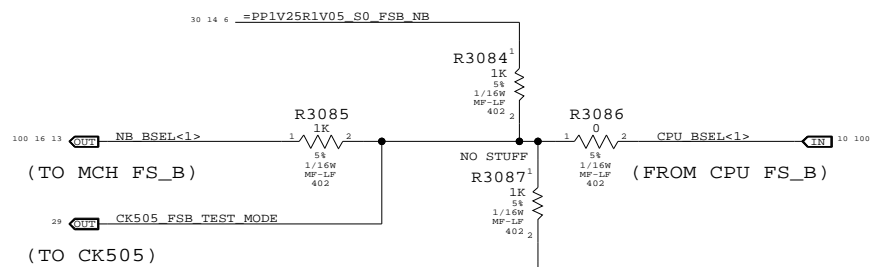
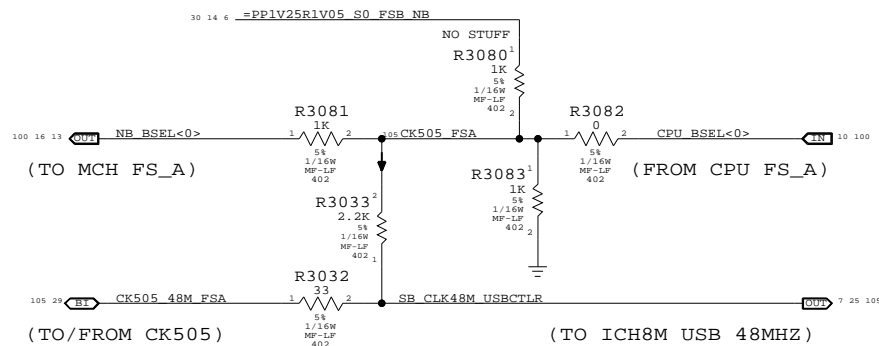
(Note: HOST/SRC/GFX clock termination kept on T9 for Cypress CY28545-5 compatibility)

CK505 Configuration Straps

FCT_SEL (GFX clock select)



FS_A, FS_B, FS_C (Host clock freq select)

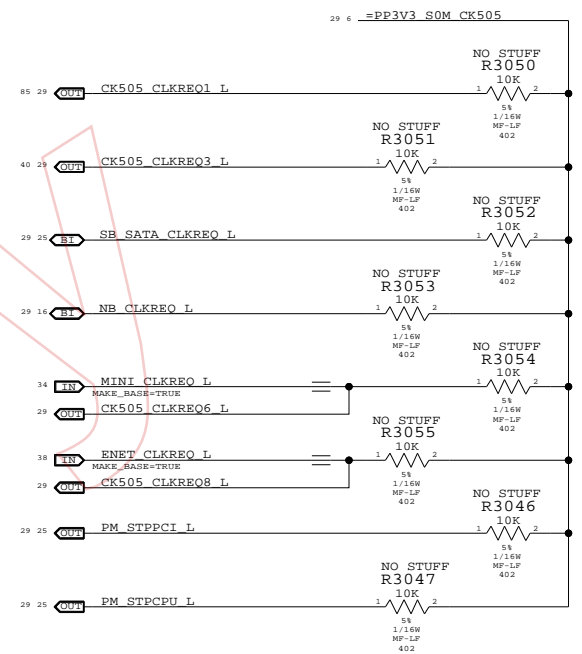


FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

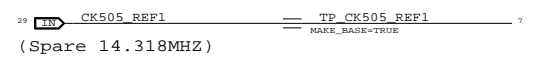
NO STUFF R3082, R3086 & R3090
for manual CPU clk frequency.

CLKREQ Controls

Silego SL8GLP537 has internal
PULL-UPS ON ALL CLKREQ# PINS?



Unused Clocks



Clock Termination

SYNC_MASTER=JAMES

SYNC_DATE=10/18/2006	7
----------------------	---

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APPLE COMPUTER INC.

SIZE
D

DRAWING NUMBER	051-
----------------	------

33

SCALE	
	NONE

SHT	3
-----	---

SHT	30
-----	----

30 °

Power aliases required by this page:

- =PP1V8_S3_MEM
- =PP0V9_S3_MEM_VREF
- =PPSPD_S0_MEM (2.5V - 3.3V)

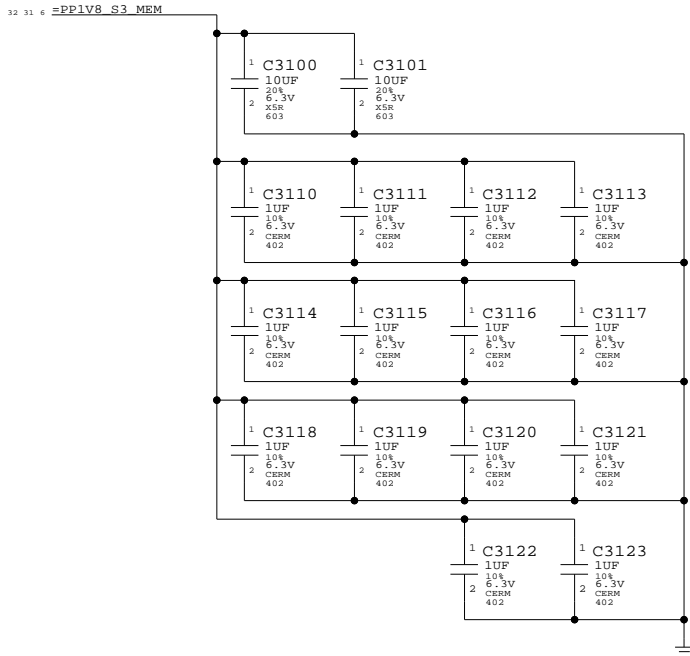
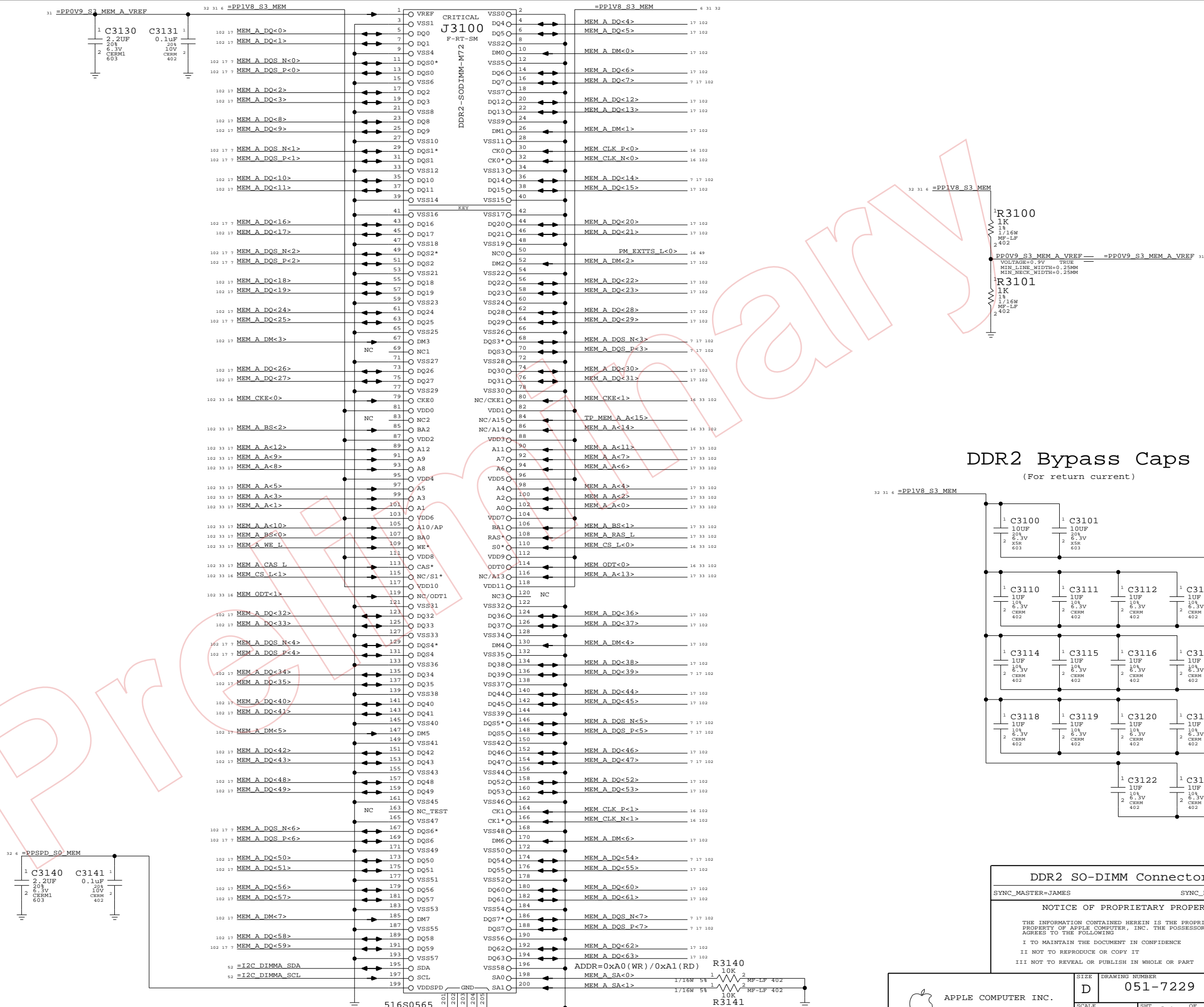
Signal aliases required by this page:

- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:

(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.



SYNC_MASTER=JAMES	SYNC_DATE=10/17/06
-------------------	--------------------

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	SIZE	DRAWING NUMBER
--	------	----------------

D	051-7229
---	----------



APPLE COMPUTER INC.

D	051-
---	------

[illegible]

SCALE	SHT 31 OF 118
-------	---------------

NONE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99
------	---	---	---	---	---	---	---	---	---	---	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----

Power aliases required by this page:

- =PPLV8_S3_MEM
- =PP0V9_S3_MEM_VREF
- =PPSPD_S0_MEM (2.5V - 3.3V)

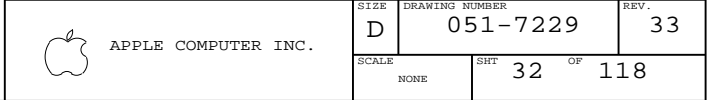
Signal aliases required by this page:

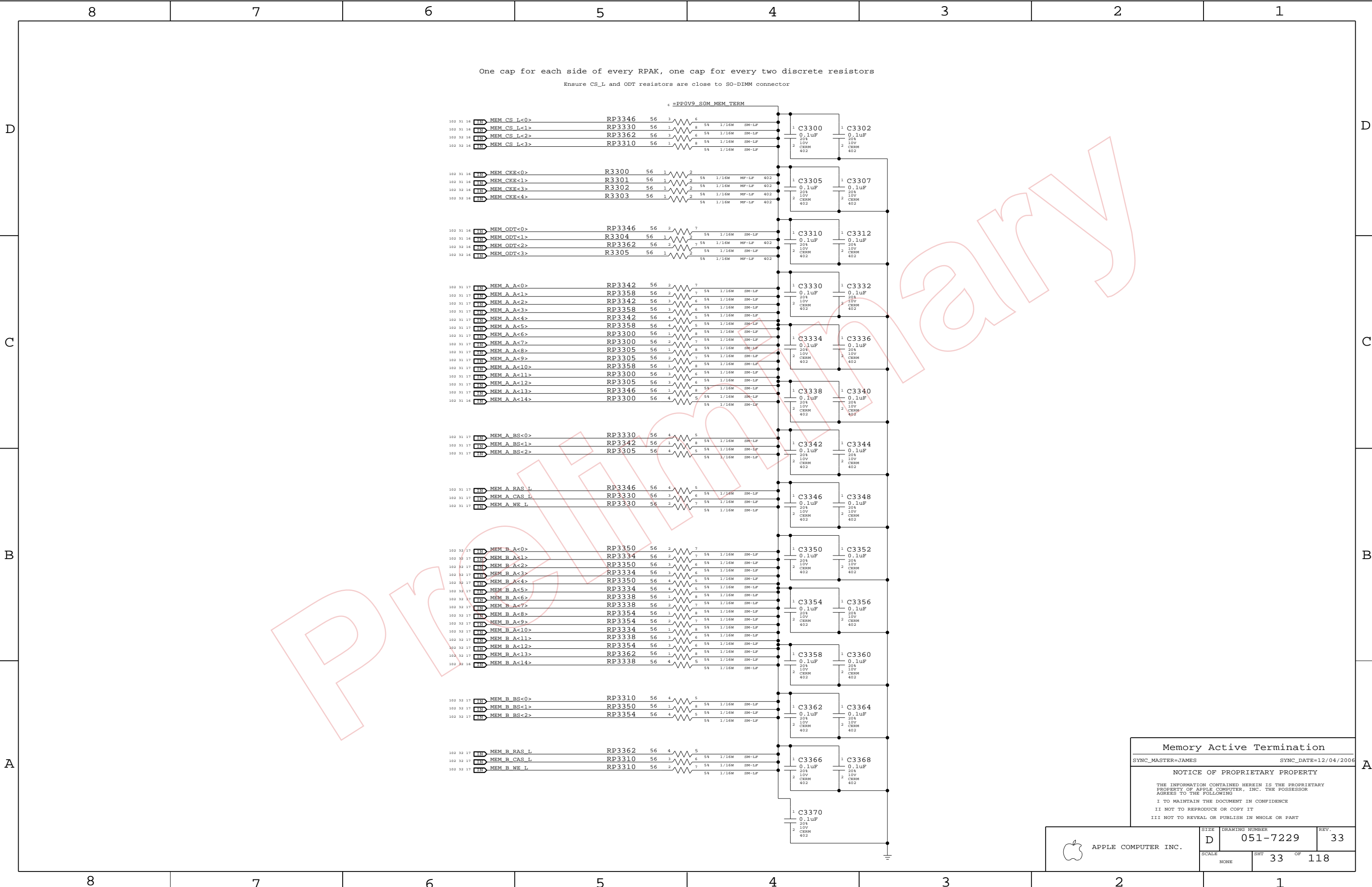
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:

(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.





Memory Active Termination

SYNC_MASTER=JAMES SYNC_DATE=12/04/2006

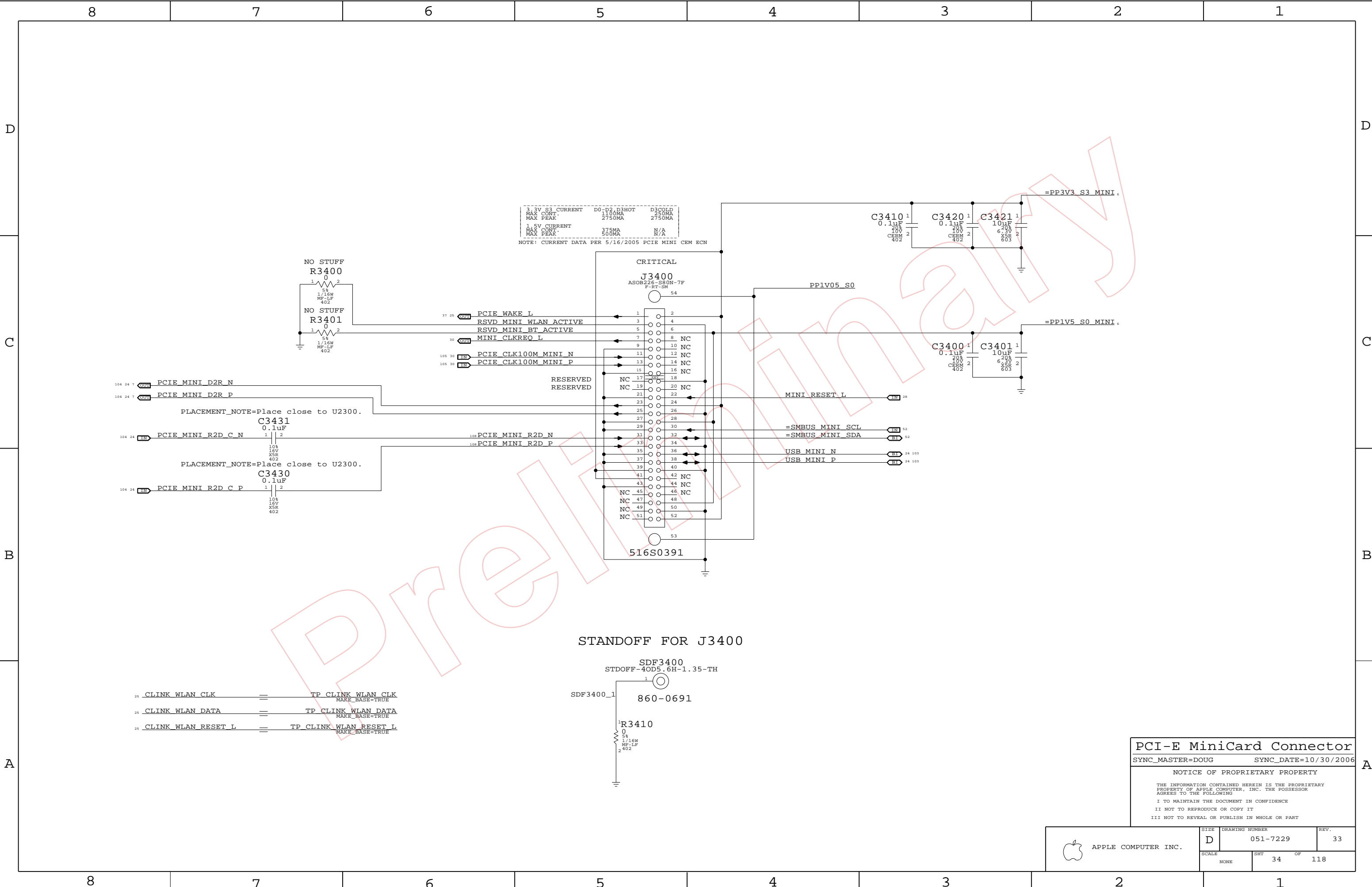
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3.3V S3 CURRENT	D0-D2, D3HOT	D3COLD
MAX. CONT.	1100MA	250MA
MAX. PEAK	2750MA	2750MA
1.5V CURRENT	375MA	N/A
MAX. CONT.	500MA	N/A
MAX. PEAK		

NOTE: CURRENT DATA PER 5/16/2005 PCIE MINI CEM ECN

STANDOFF FOR J3400

SDF3400
STDOFF-40D5.6H-1.35-TH

860-0691

R3410

0 5%
1/16W
MF-LF
2 402

PCI-E MiniCard Connector

SYNC_MASTER=DOUG SYNC_DATE=10/30/2006

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE	SHT	OF
NONE	34	118


D

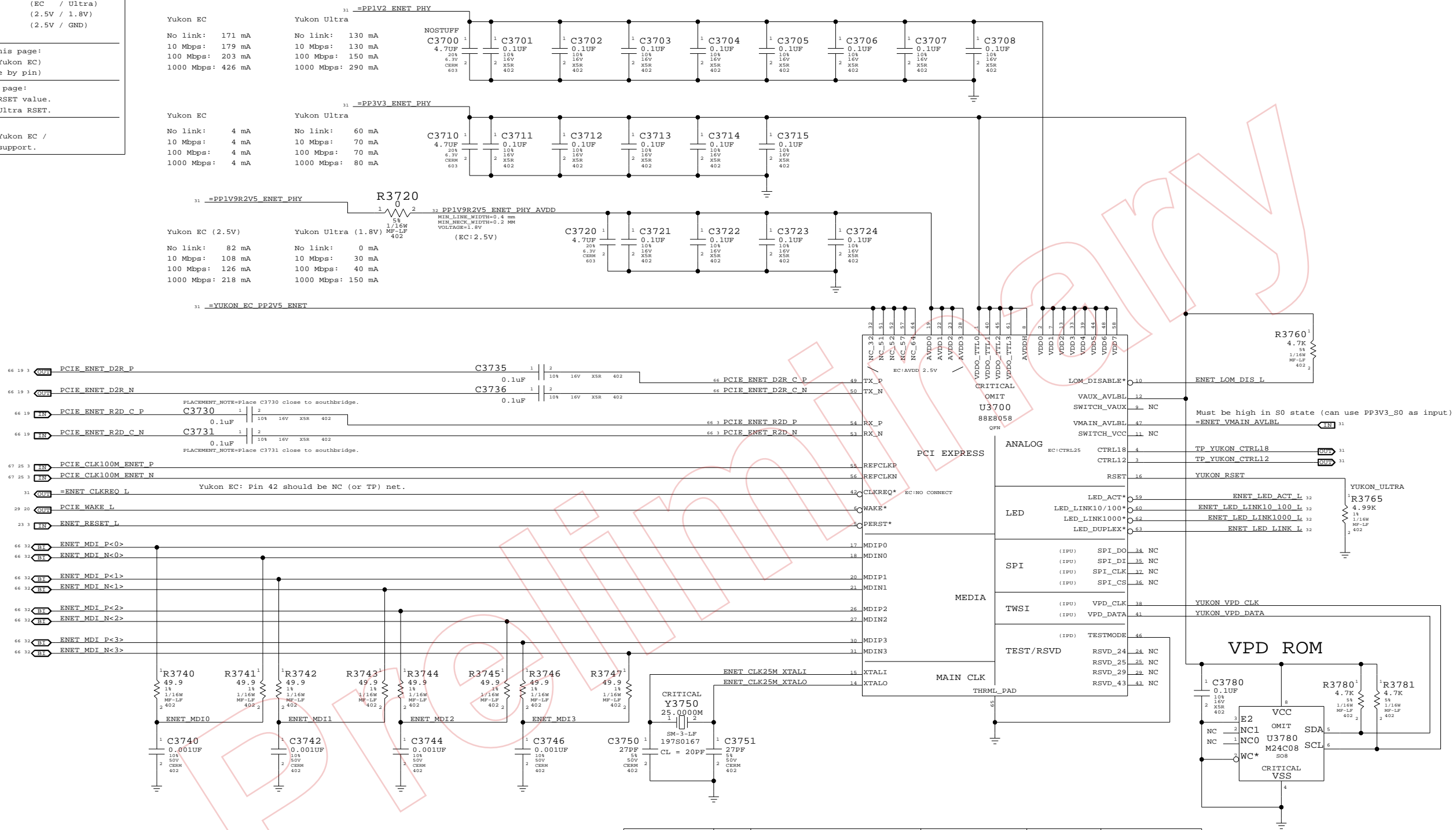
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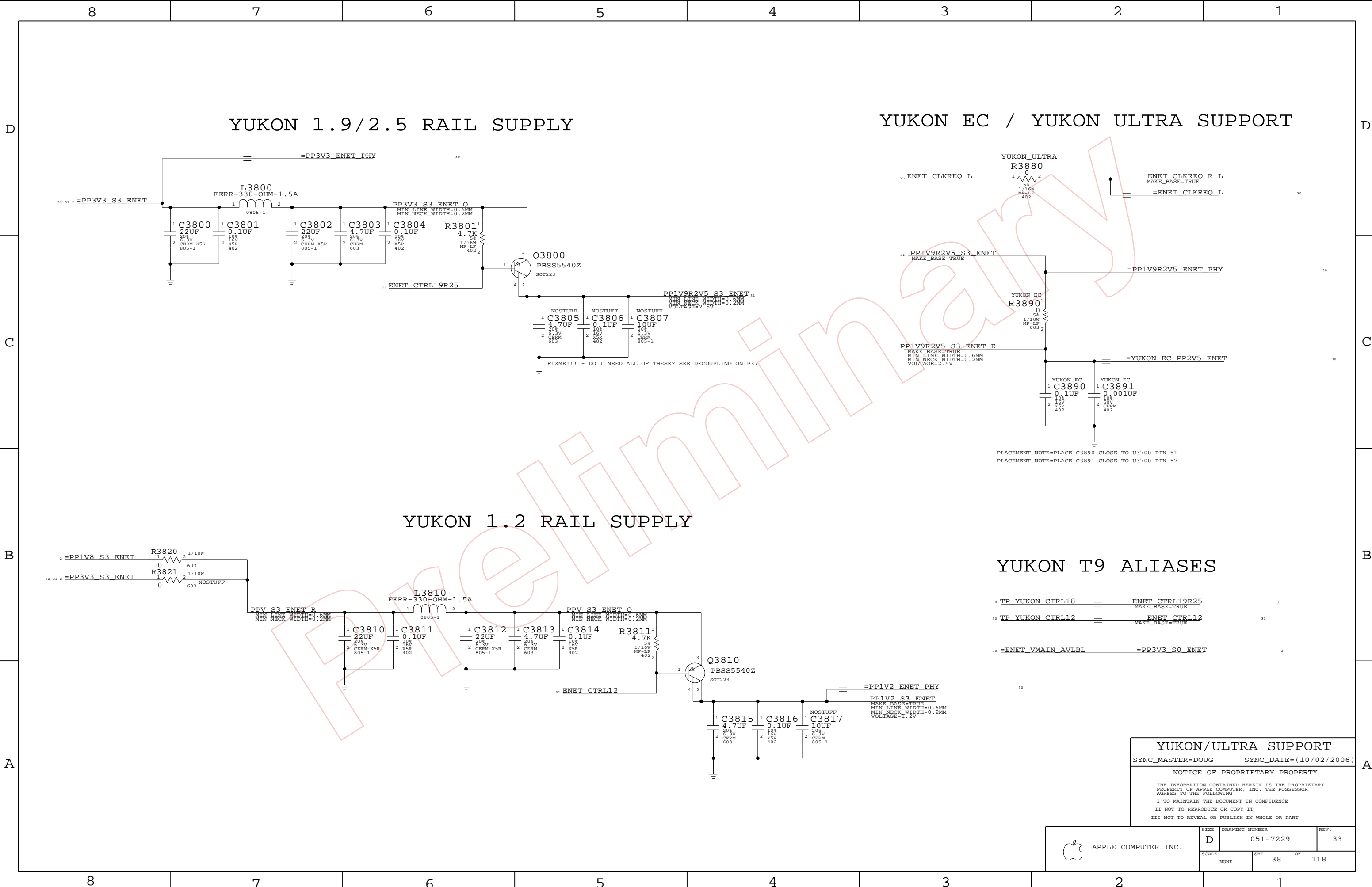
B

A

Ethernet (Yukon)	
SYNC_MASTER=DOUG	SYNC_DATE=11/08/2006
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7229	33
	SCALE	SHT OF	
	NONE	37 118	



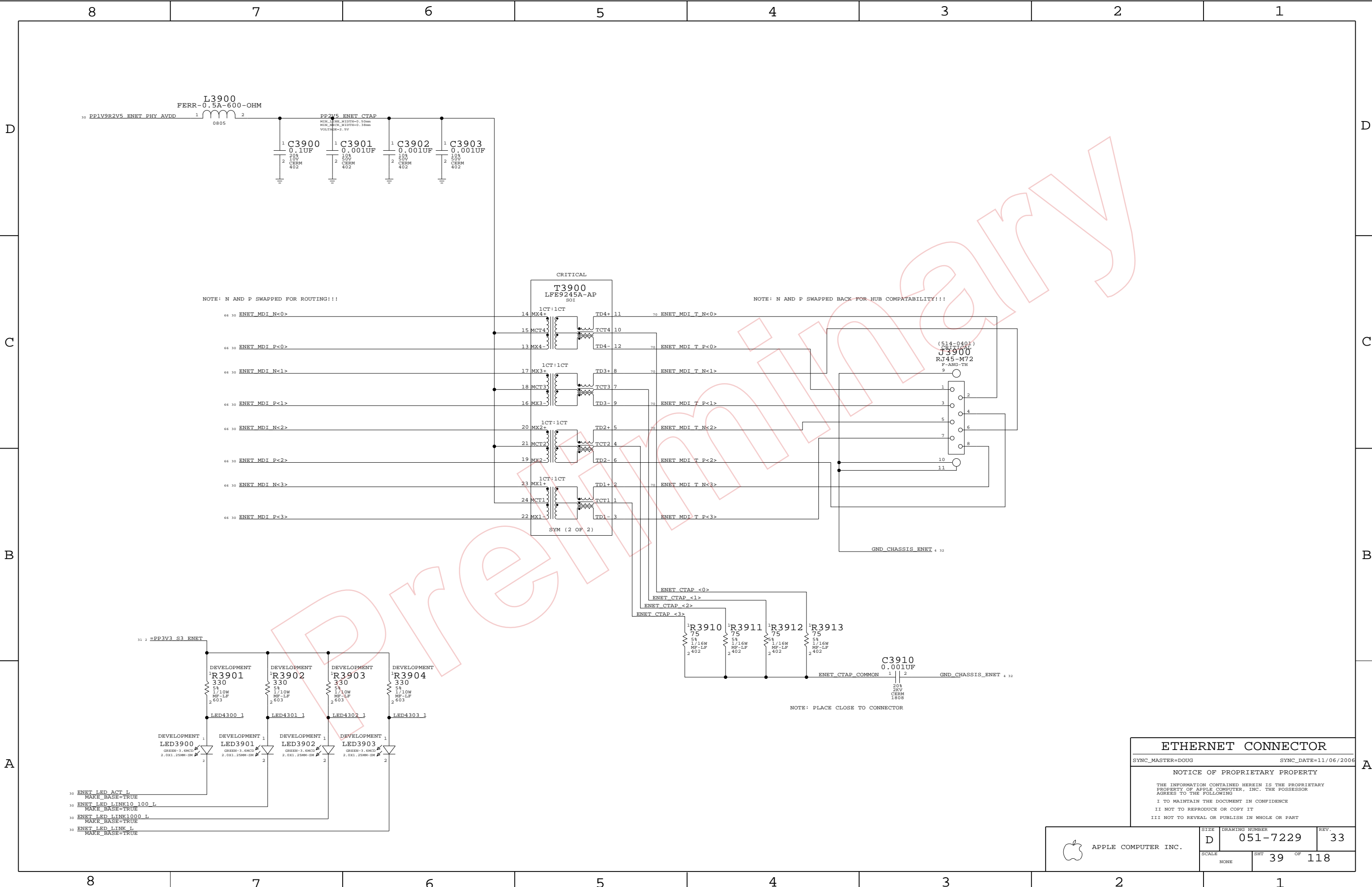


YUKON T9 ALIASES

TP YUKON_CTRL18 = ENET_CTRL19R25
TP YUKON_CTRL12 = ENET_CTRL12
=ENET_VMAIN_AVLBL = =PP3V3_S0_ENET

YUKON/ULTRA SUPPORT
SYNC_MASTER=DOUG SYNC_DATE=(10/02/2006)
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7229	REV. 33
	SCALE NONE	SHT 38	OF 118



ETHERNET CONNECTOR

SYNC_MASTER=DOUG

SYNC_DATE=11/06/2006

NOTICE OF PROPRIETARY PROPERTY

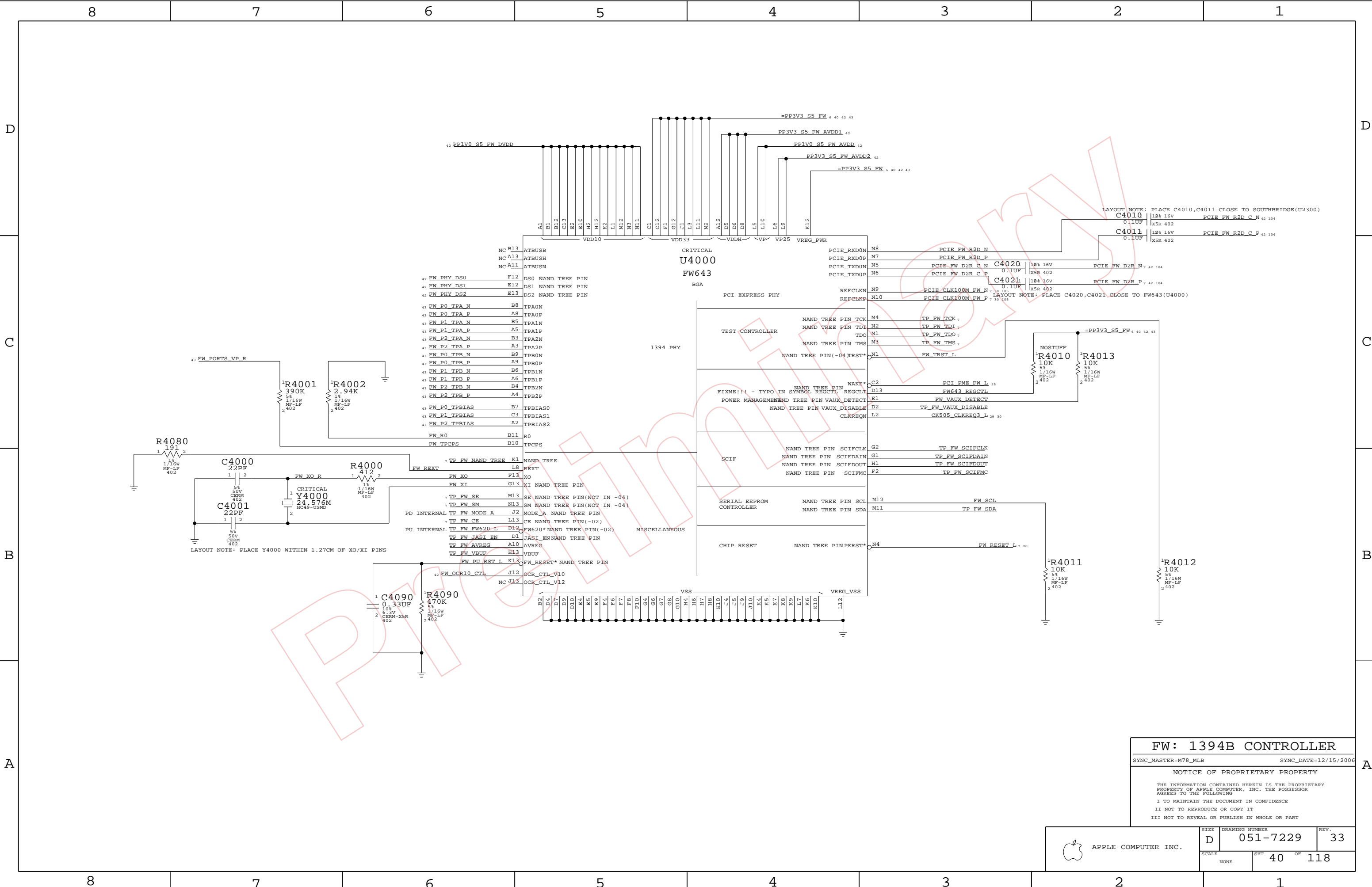
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	D	051-7229	33
SCALE		SHT	OF
NONE		39	118



FW: 1394B CONTROLLER

SYNC_MASTER=M78_MLB SYNC_DATE=12/15/2006

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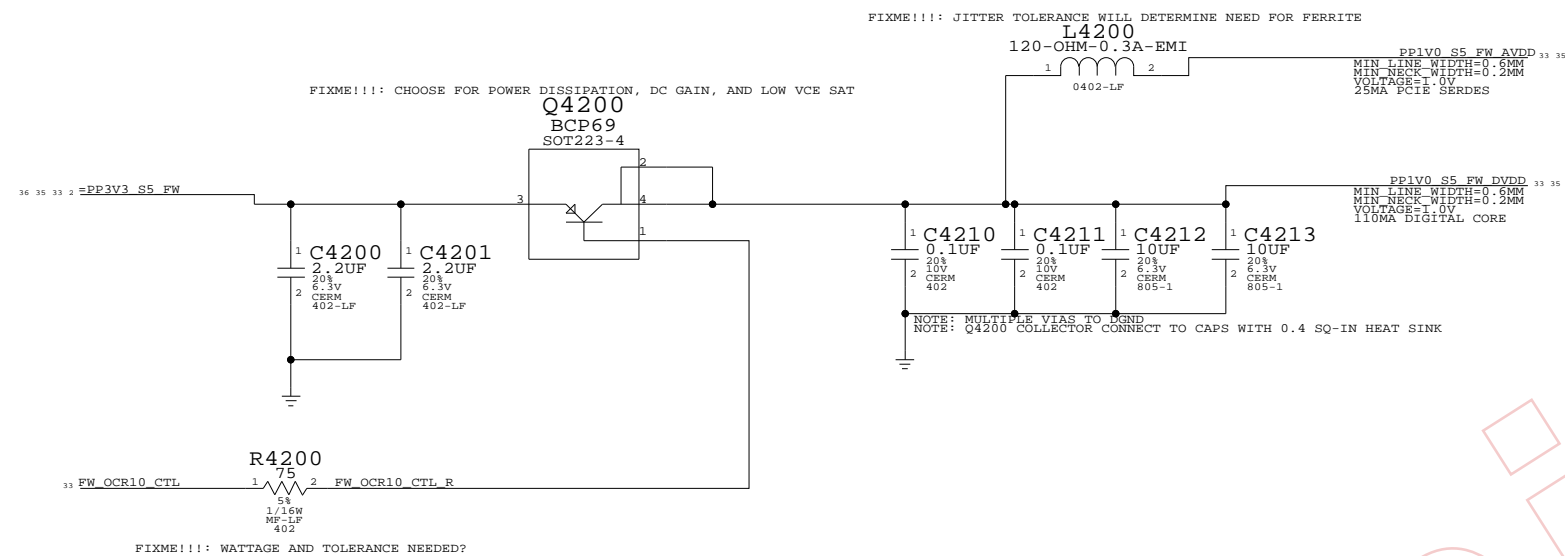
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7229	33
SCALE		SHT	OF
NONE		40	118

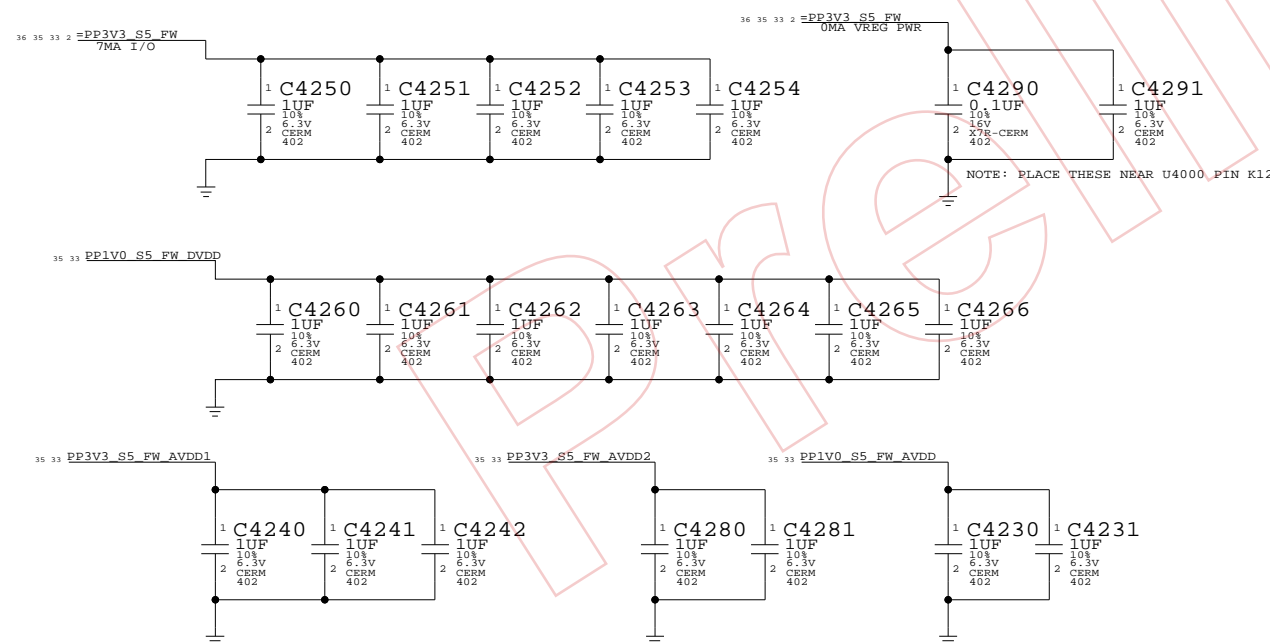


FW643 1.0V GENERATION

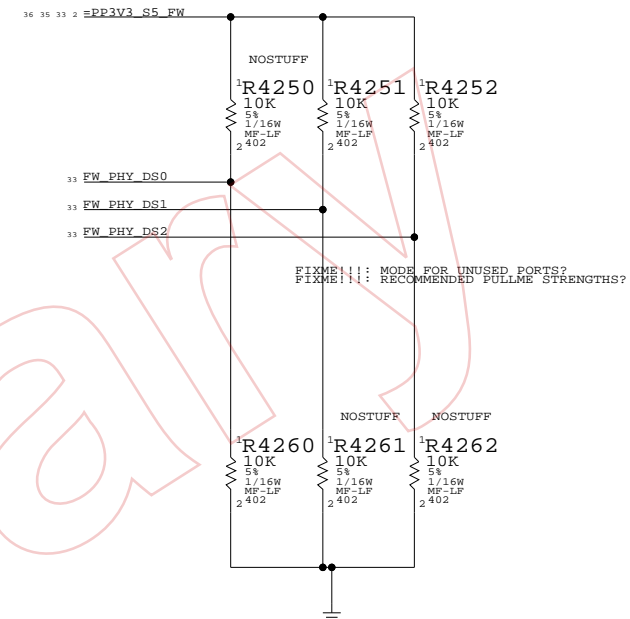


FW643 DECOUPLING

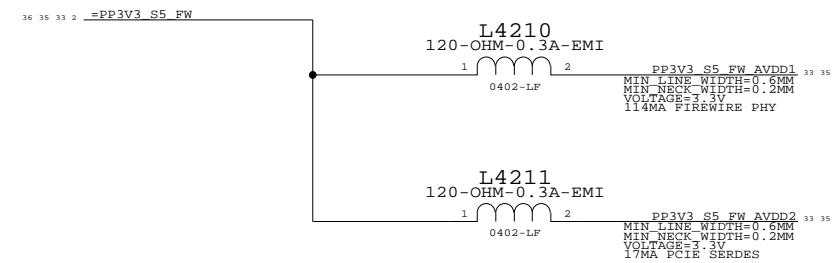
NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4000



1394 PHY DATA/STROBE OPTIONS



FW 3.3V FILTERING



FW PCIE ALIASES

	19	TP_PCIE_FW_R2D_C_N	==	PCIE_FW_R2D_C_N MAKE_BASE=TRUE	33
	19	TP_PCIE_FW_R2D_C_P	==	PCIE_FW_R2D_C_P MAKE_BASE=TRUE	33
33	3	PCIE_FW_D2R_N MAKE_BASE=TRUE	==	TP_PCIE_FW_D2R_N	1
33	3	PCIE_FW_D2R_P MAKE_BASE=TRUE	==	TP_PCIE_FW_D2R_P	1

FW: 1394B MISC

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SYNC_MASTER=DOUG

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SYNC_DATE=10/10/2006	7
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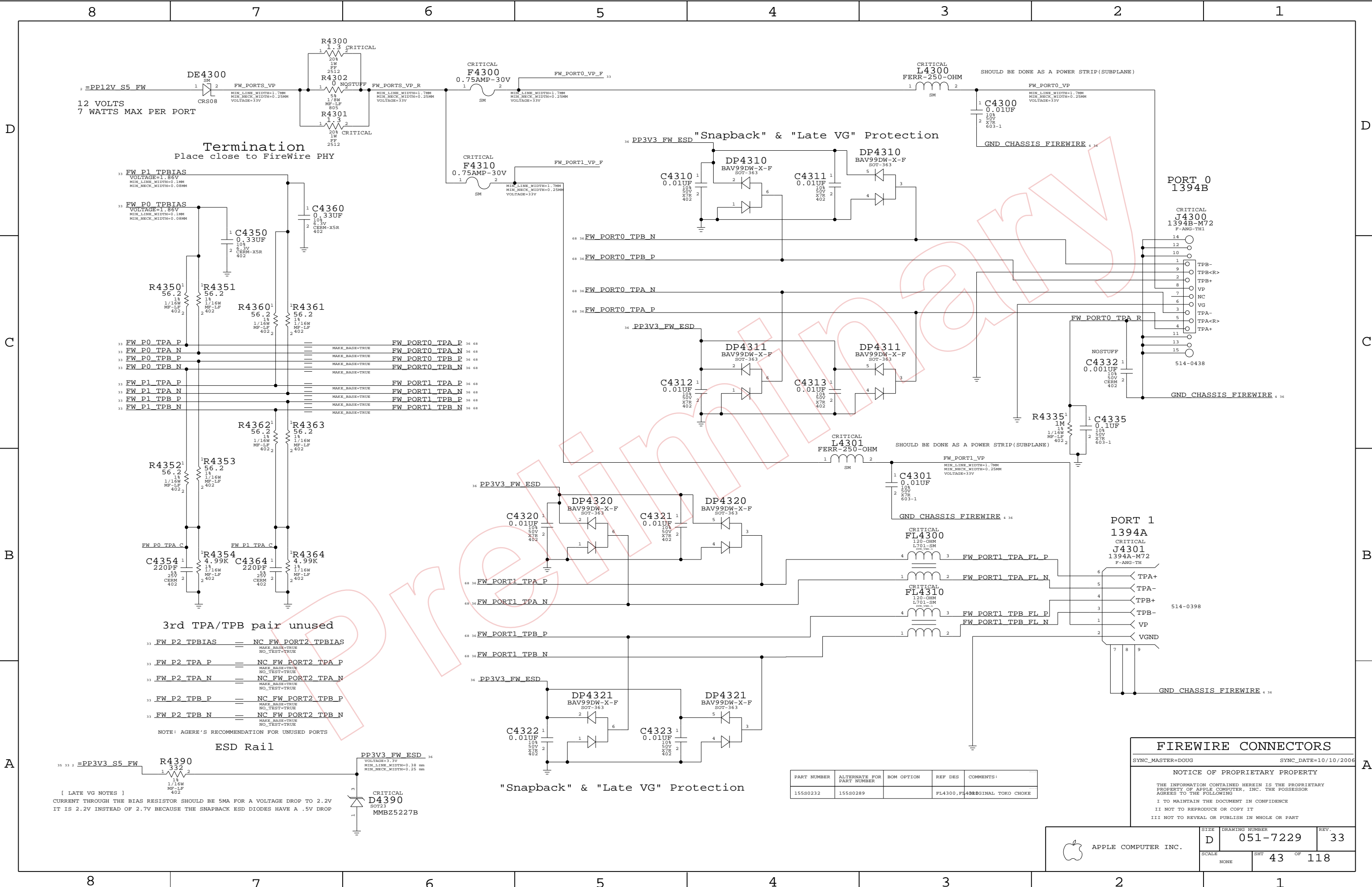
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APPLE COMPUTER INC.

SIZE D	DRAWING NUMBER 051-7229	REV. 33
SCALE NONE	SHT 42	OF 118



Termination
Place close to FireWire PHY

"Snapback" & "Late VG" Protection

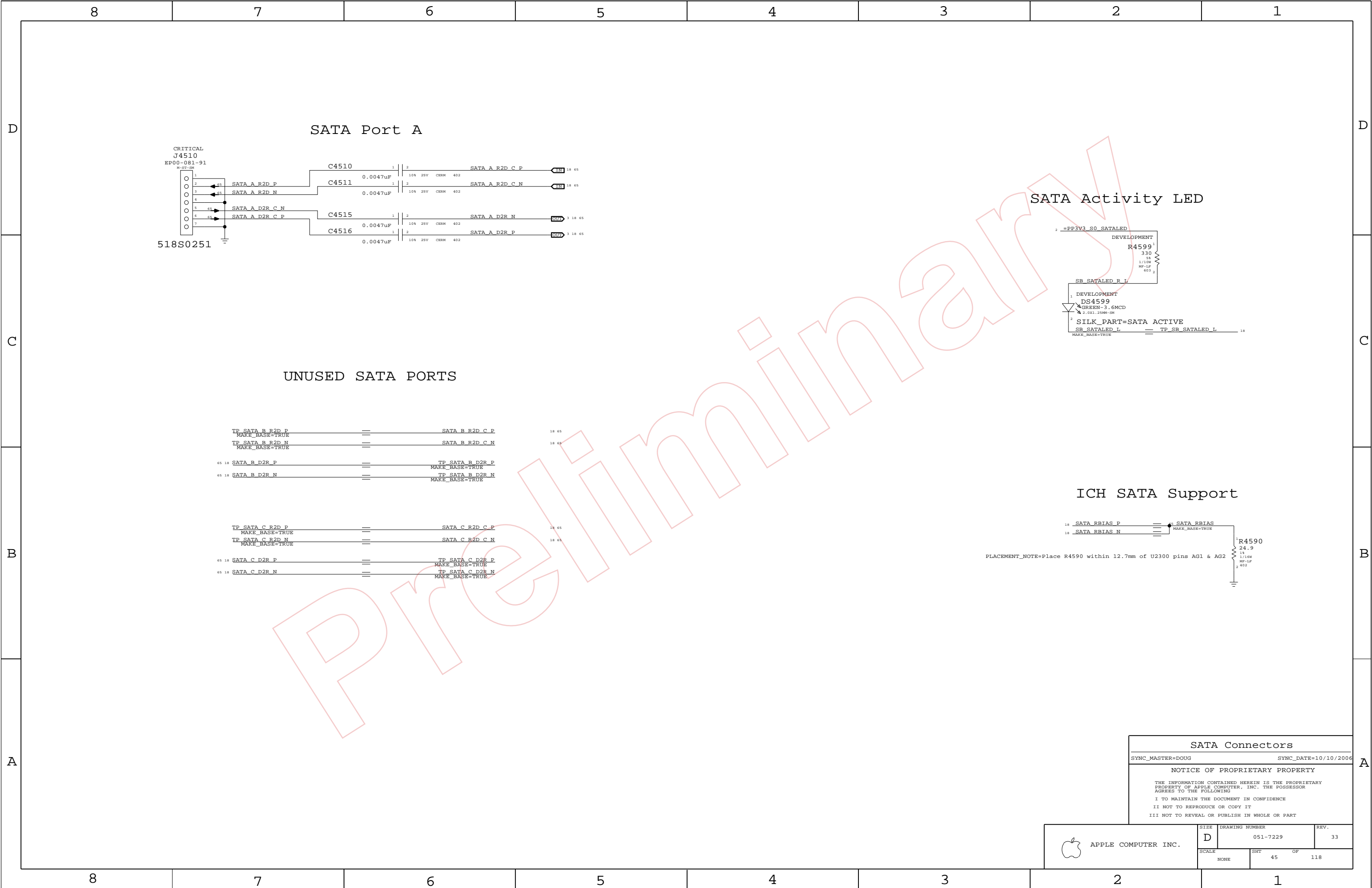
3rd TPA/TPB pair unused

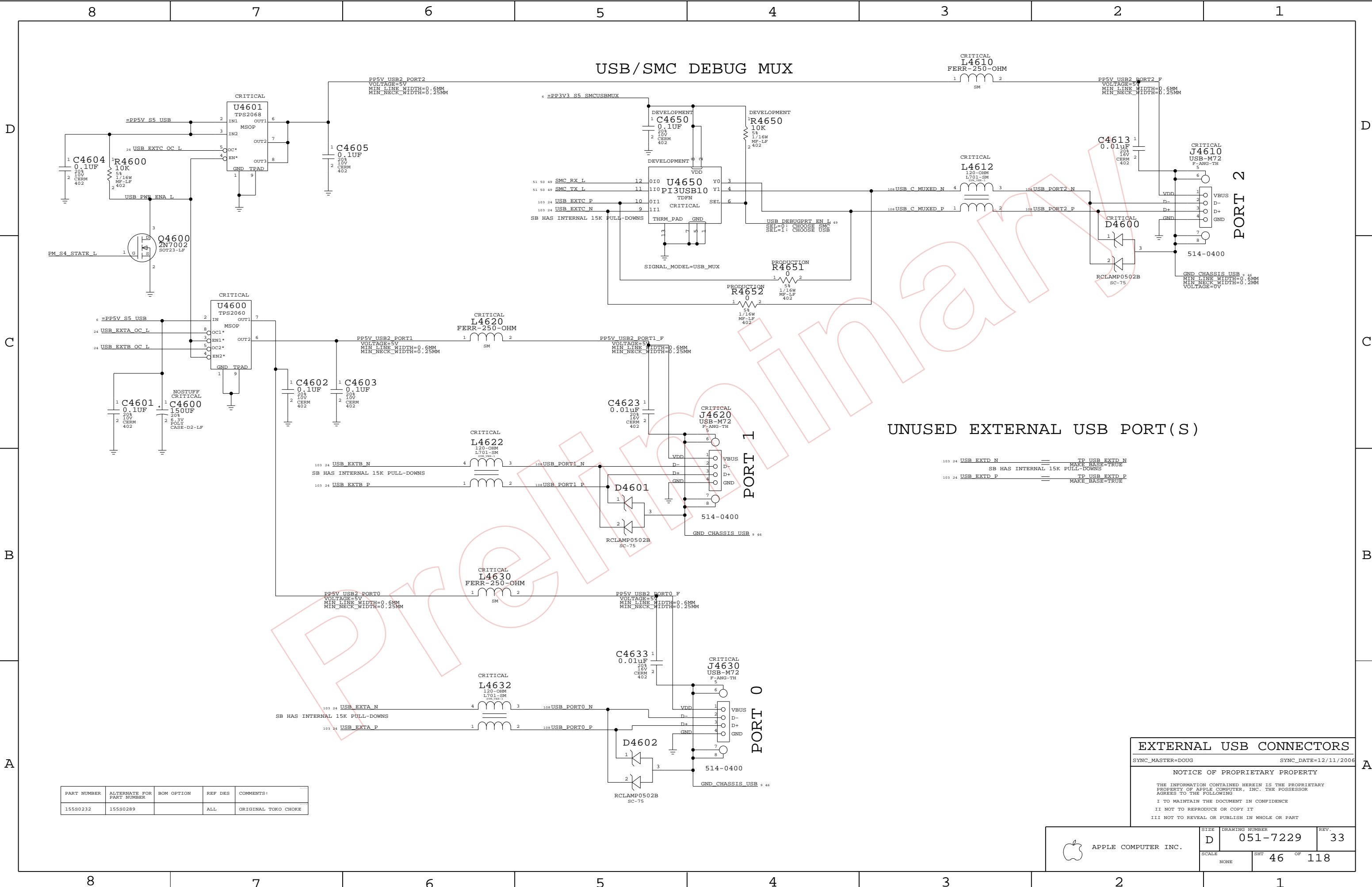
"Snapback" & "Late VG" Protection

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
155S0232	155S0289		FL4300, FL4310	49REGINAL TOKO CHOKE

FIREWIRE CONNECTORS	
SYNC_MASTER=DOUG	SYNC_DATE=10/10/2006
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	D	051-7229	33
SCALE		SHT	OF
NONE		43	118





PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		ALL	ORIGINAL TORO CHOKE

UNUSED EXTERNAL USB PORT(S)

103	24	USB_EXTD_N	==	TP USB_EXTD_N
				MAKE_BASE=TRUE
				SB HAS INTERNAL 15K PULL-DOWNS
103	24	USB_EXTD_P	==	TP USB_EXTD_P
				MAKE_BASE=TRUE

EXTERNAL USB CONNECTORS

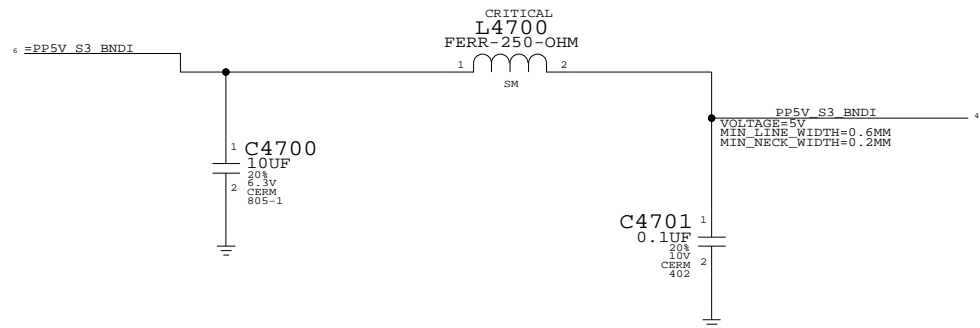
SYNC_MASTER=DOUG SYNC_DATE=12/11/2006

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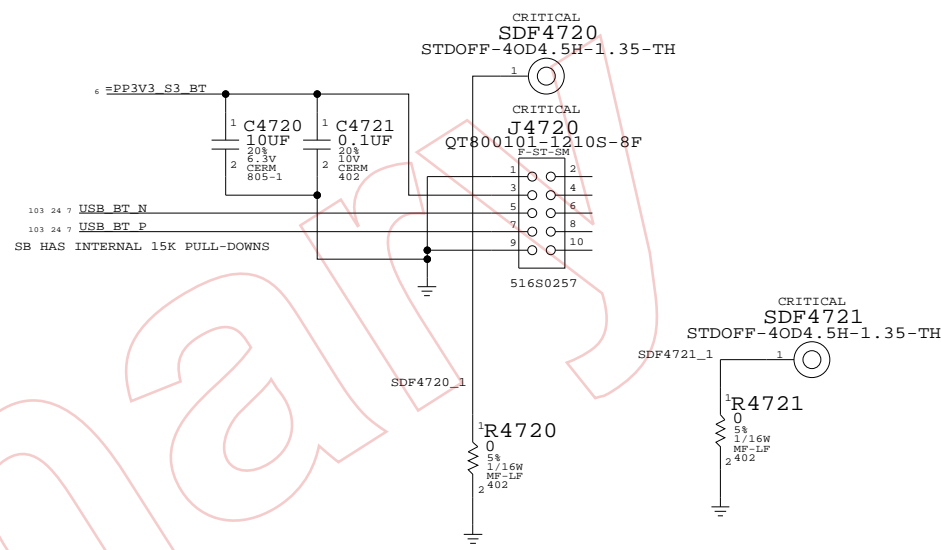
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7229	33
	SCALE	SHT	OF
	NONE	46	118

CAMERA POWER FILTERING

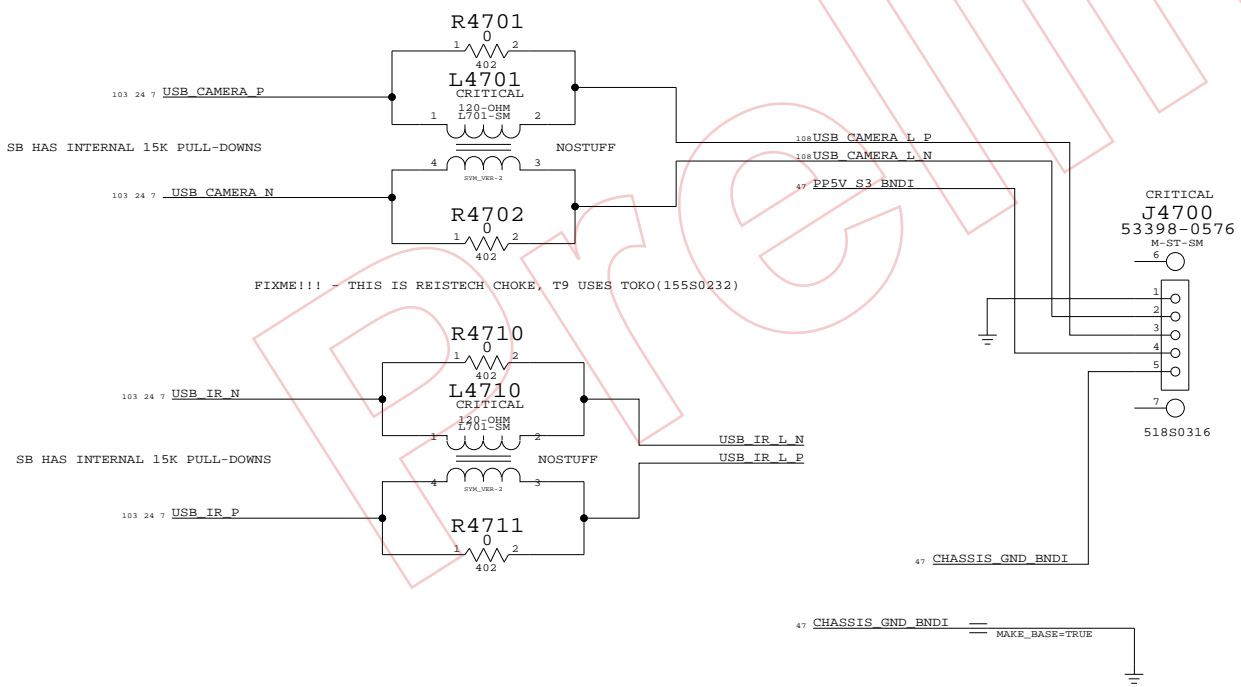


LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

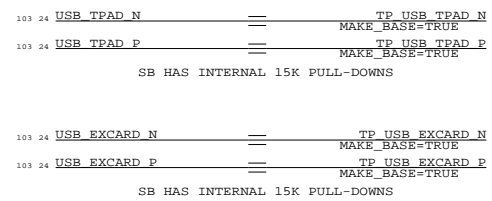
M13D (Bluetooth) Connector



CAMERA CONNECTOR

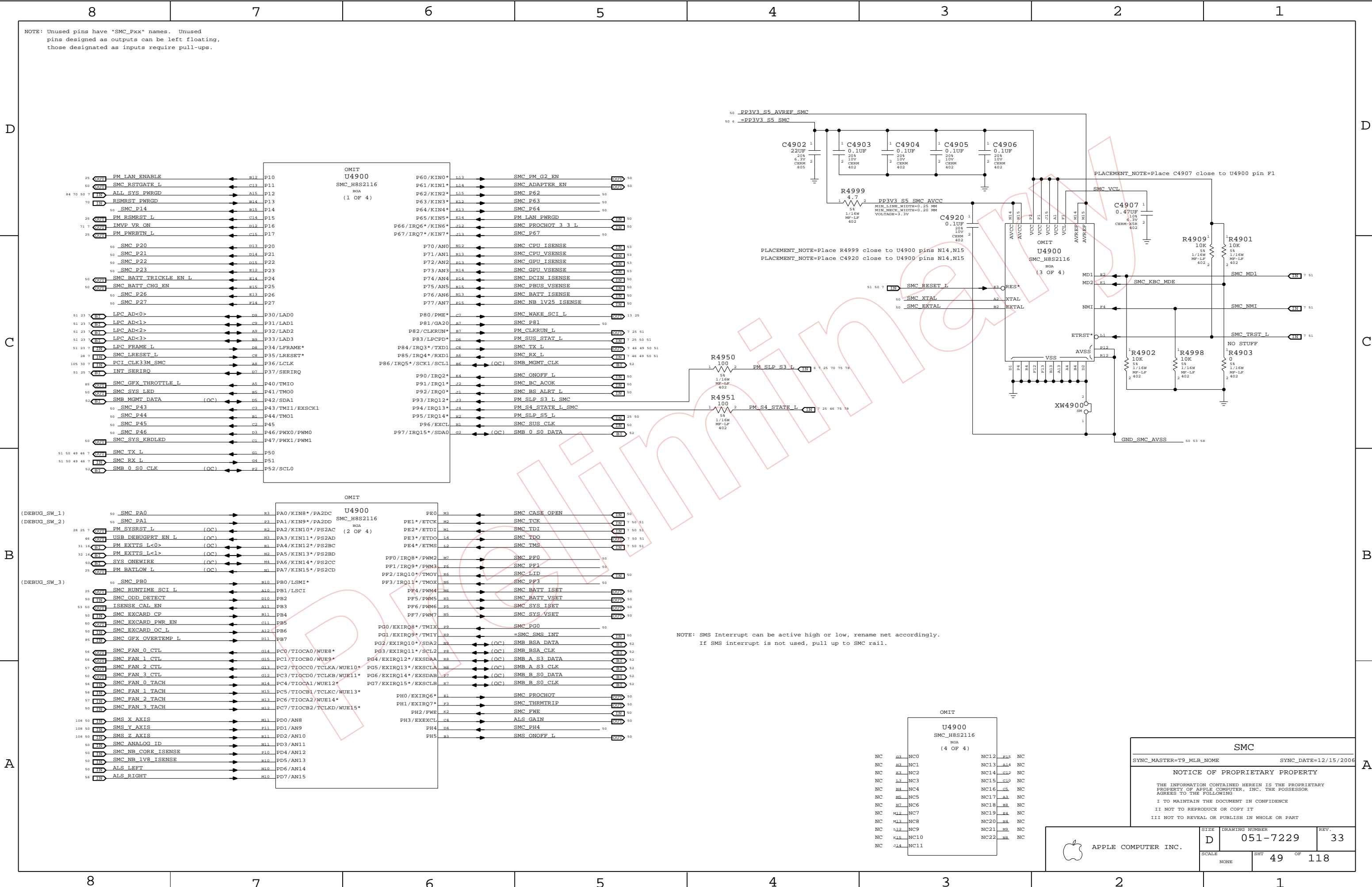


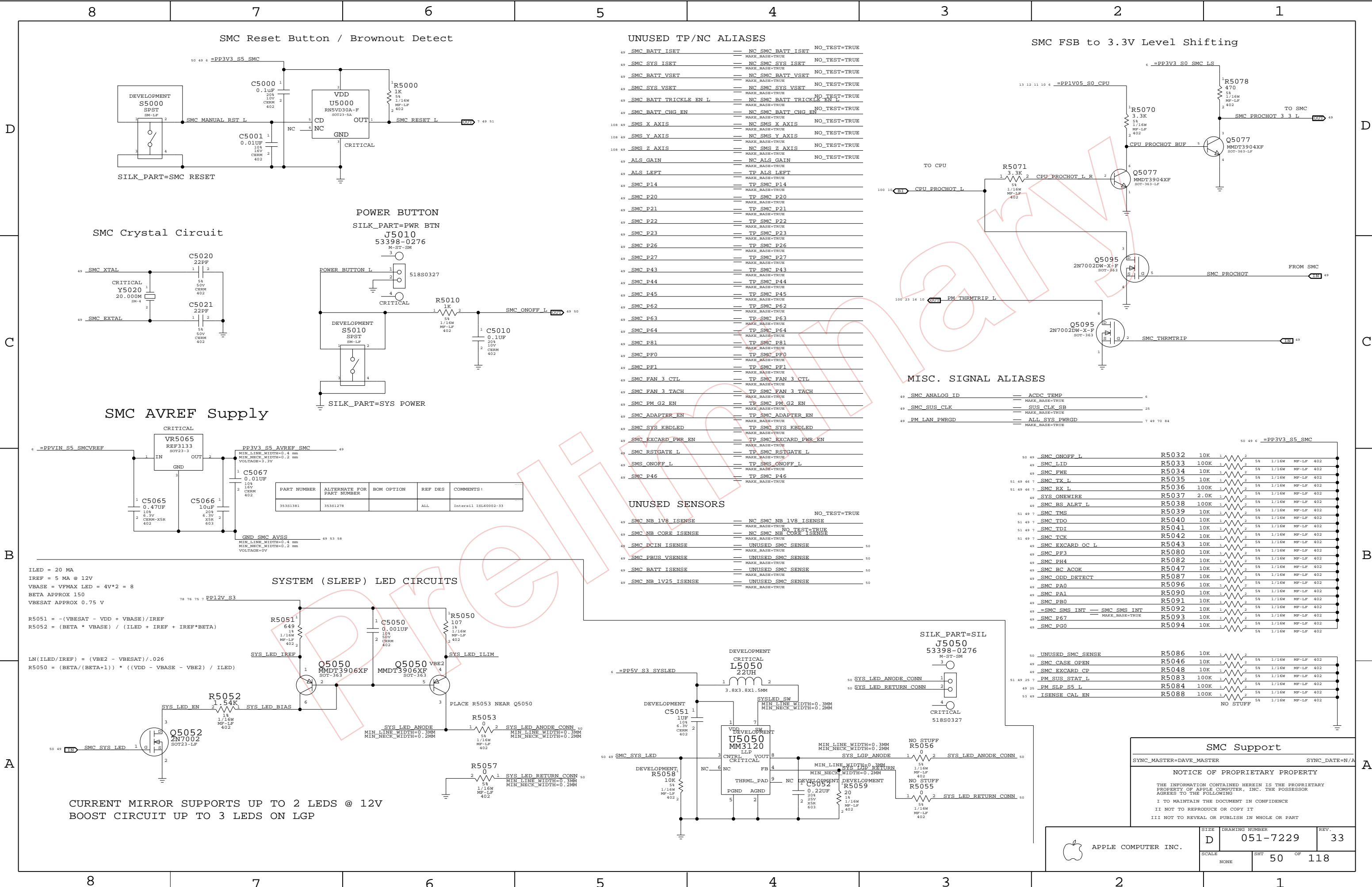
UNUSED INTERNAL USB PORTS

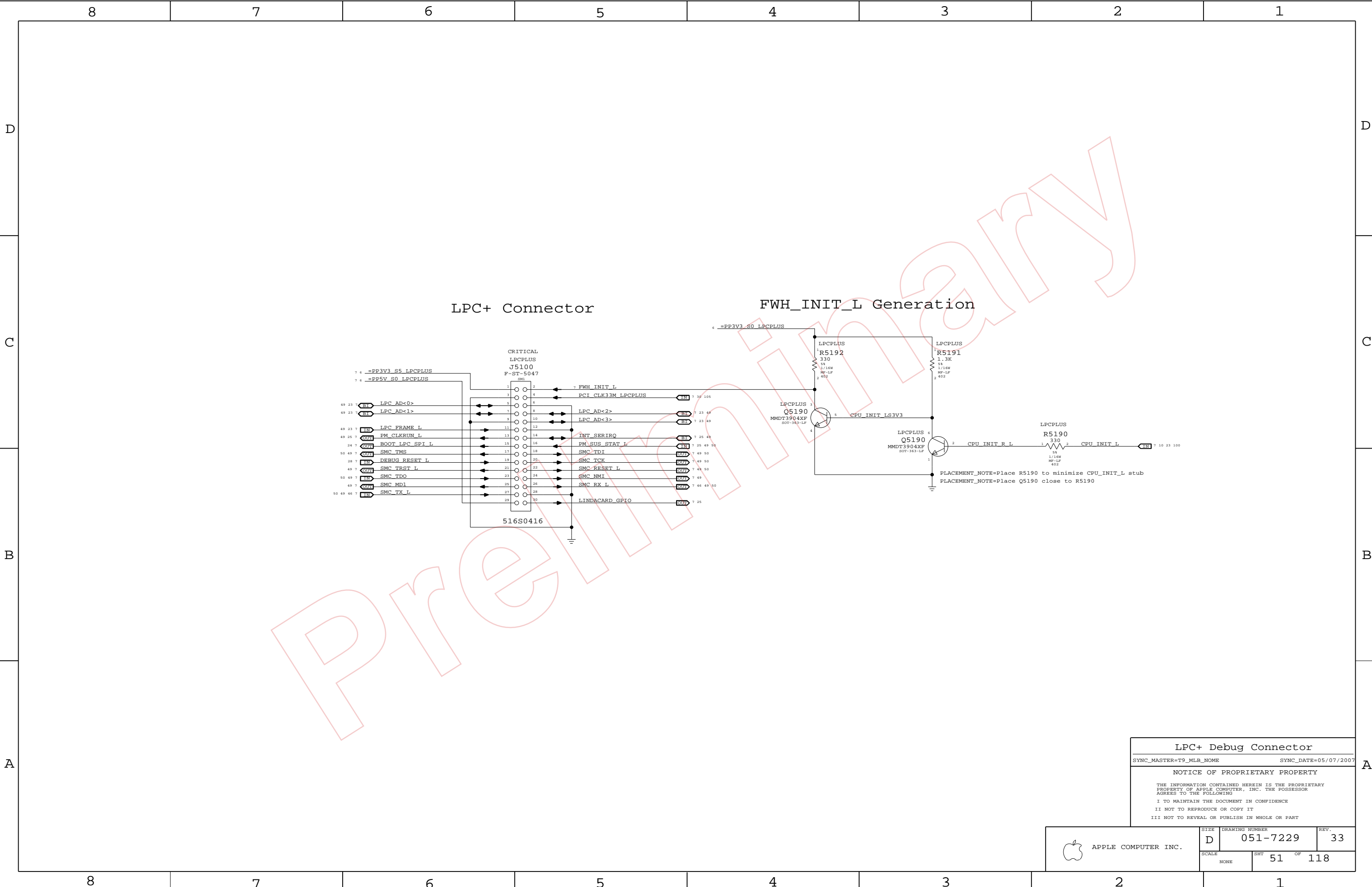


Internal USB Connections		
SYNC_MASTER=M78_MLB		SYNC_DATE=12/15/2006
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7229	REV. 33
	SCALE NONE	SHT 47	OF 118







LPC+ Debug Connector

SYNC_MASTER=T9_MLB_NONE SYNC_DATE=05/07/2007

NOTICE OF PROPRIETARY PROPERTY

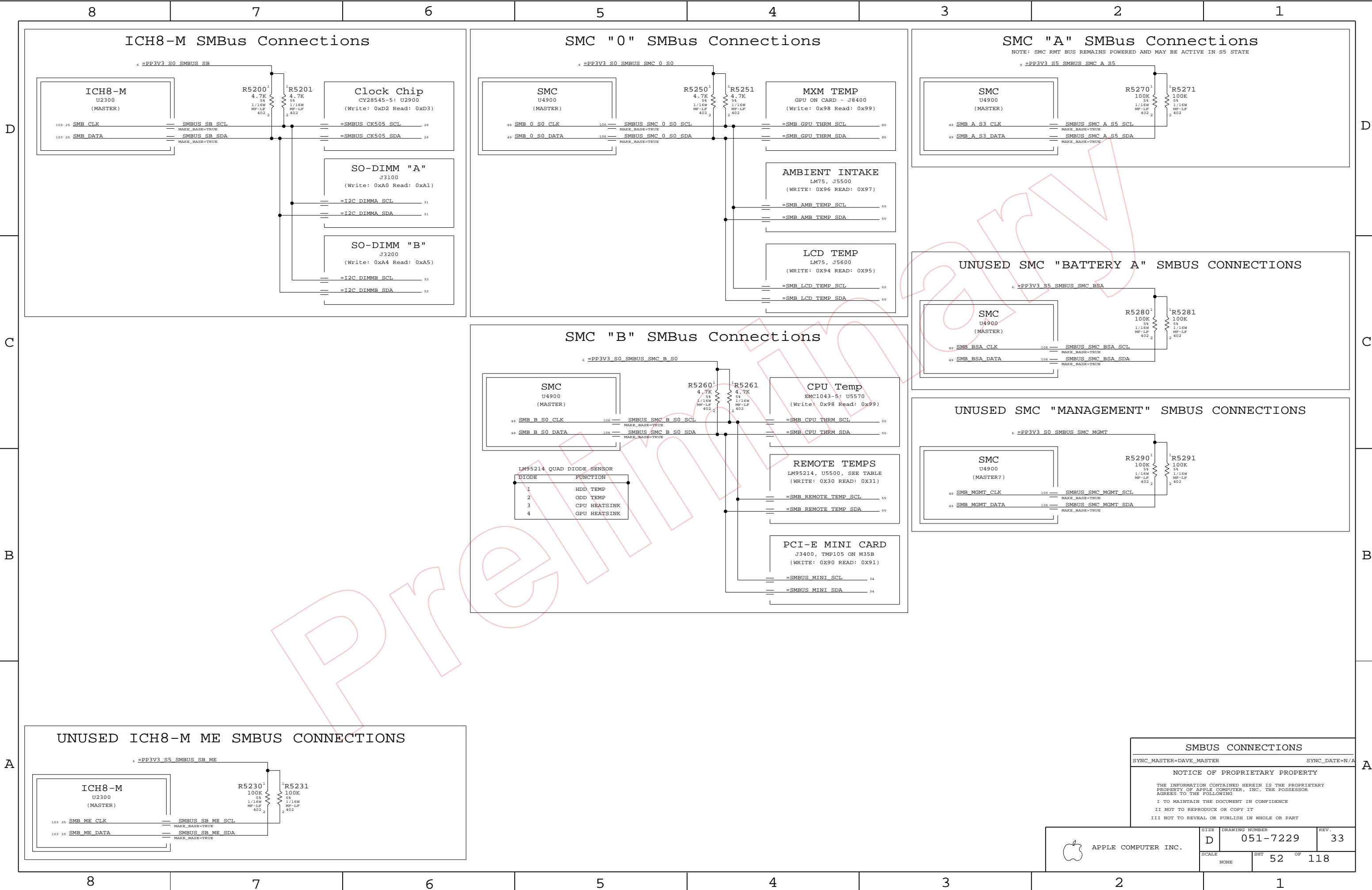
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	D	051-7229	33
SCALE		SHT	OF
NONE		51	118



SMBUS CONNECTIONS

SYNC_MASTER=DAVE_MASTER

SYNC_DATE=N/A

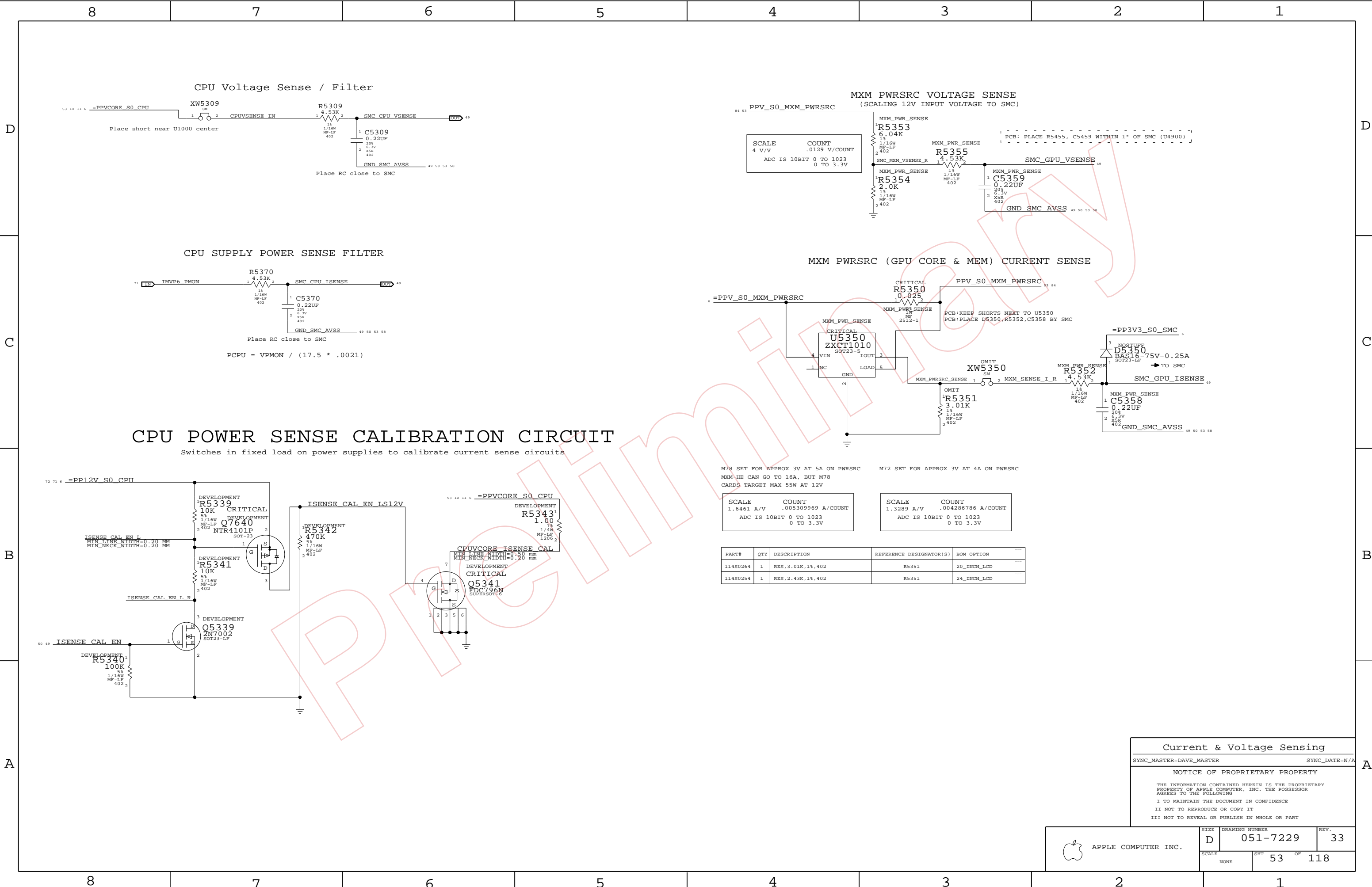
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CPU POWER SENSE CALIBRATION CIRCUIT

Switches in fixed load on power supplies to calibrate current sense circuits

M78 SET FOR APPROX 3V AT 5A ON PWRSRC
MXM-HE CAN GO TO 16A, BUT M78
CARDS TARGET MAX 55W AT 12V

SCALE	COUNT
1.6461 A/V	.005309969 A/COUNT
ADC IS 10BIT 0 TO 1023	0 TO 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BCM OPTION
114S0264	1	RES,3.01K,1%,402	R5351	20_INCH_LCD
114S0254	1	RES,2.43K,1%,402	R5351	24_INCH_LCD

Current & Voltage Sensing

SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

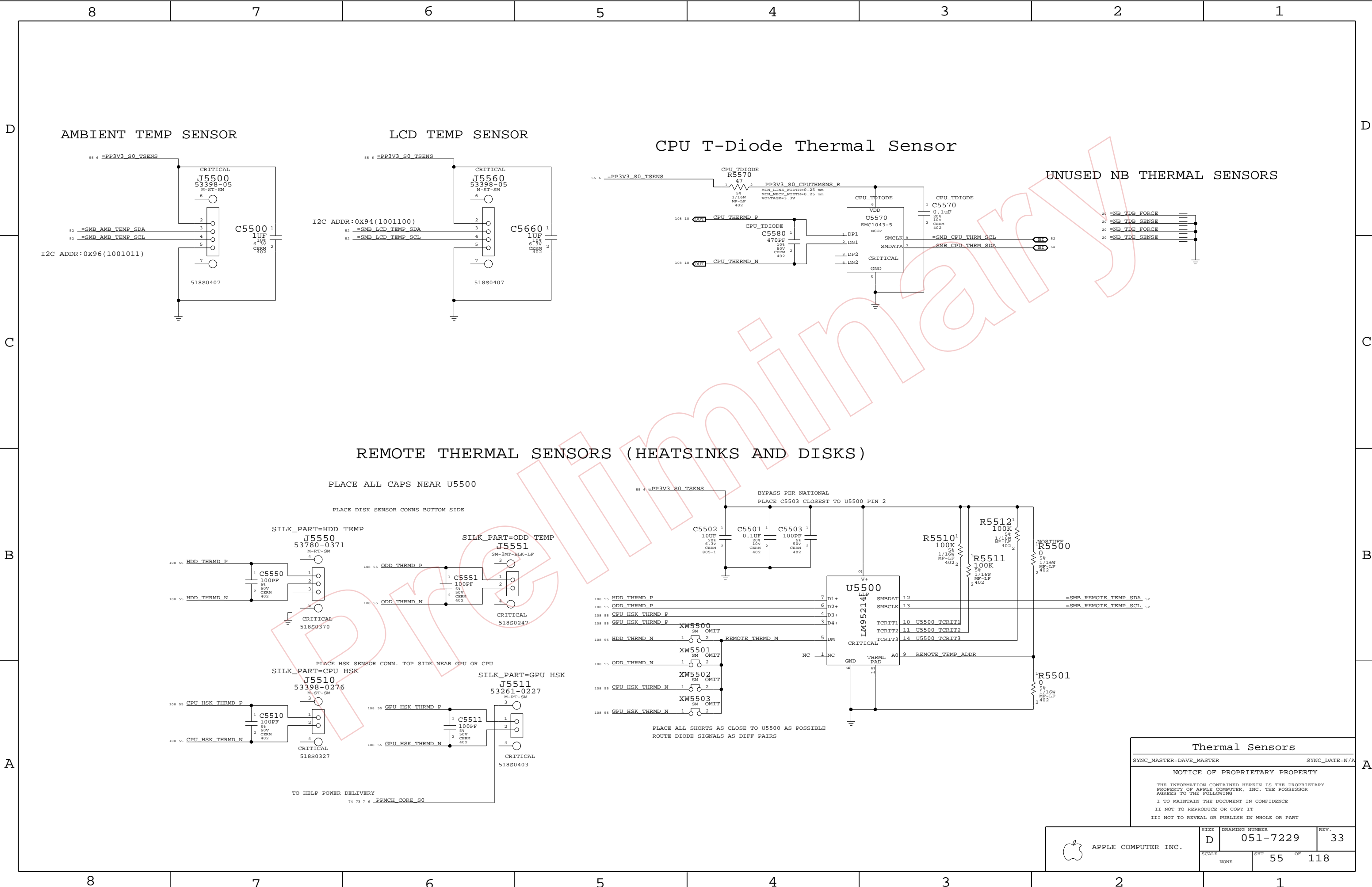
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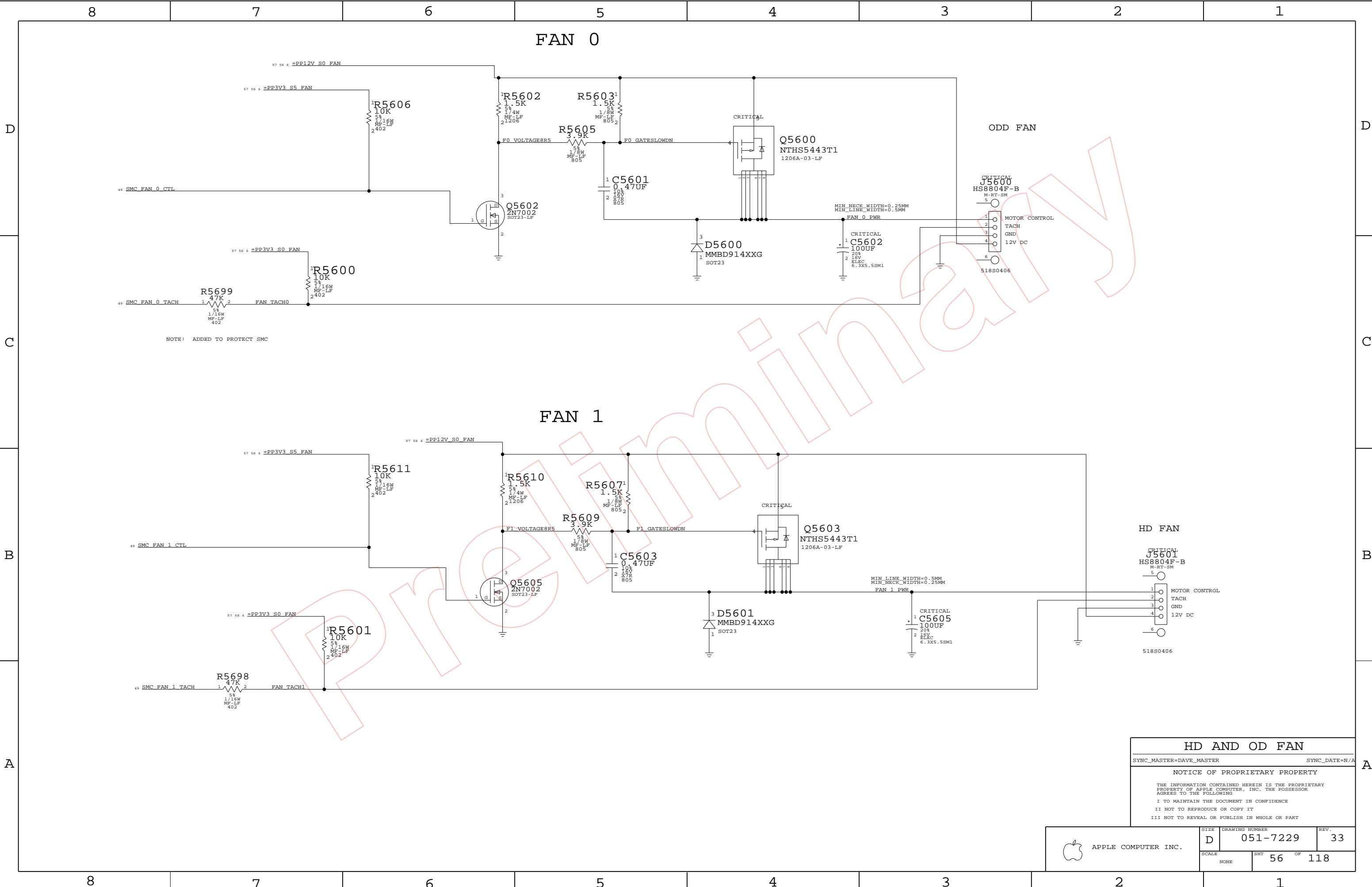
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7229	33
SCALE	NONE	SHT	53 OF 118



Thermal Sensors		
SYNC_MASTER=DAVE_MASTER		SYNC_DATE=N/A
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7229	33
SCALE		SHT	OF
NONE		55	118



HD AND OD FAN

SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

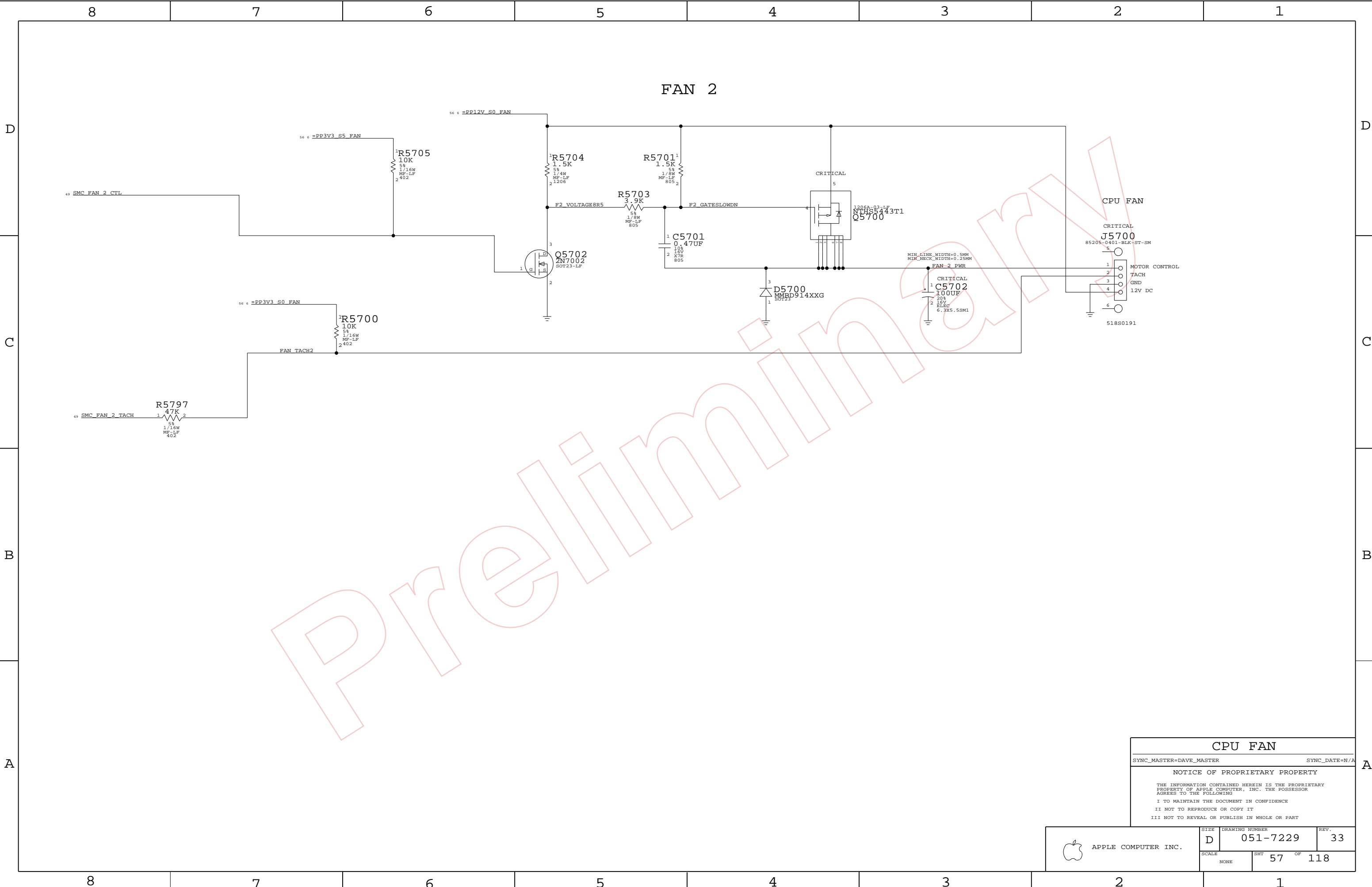
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7229	33
SCALE		SHT	OF
NONE		56	118



CPU FAN

SYNC_MASTER=DAVE_MASTER

SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

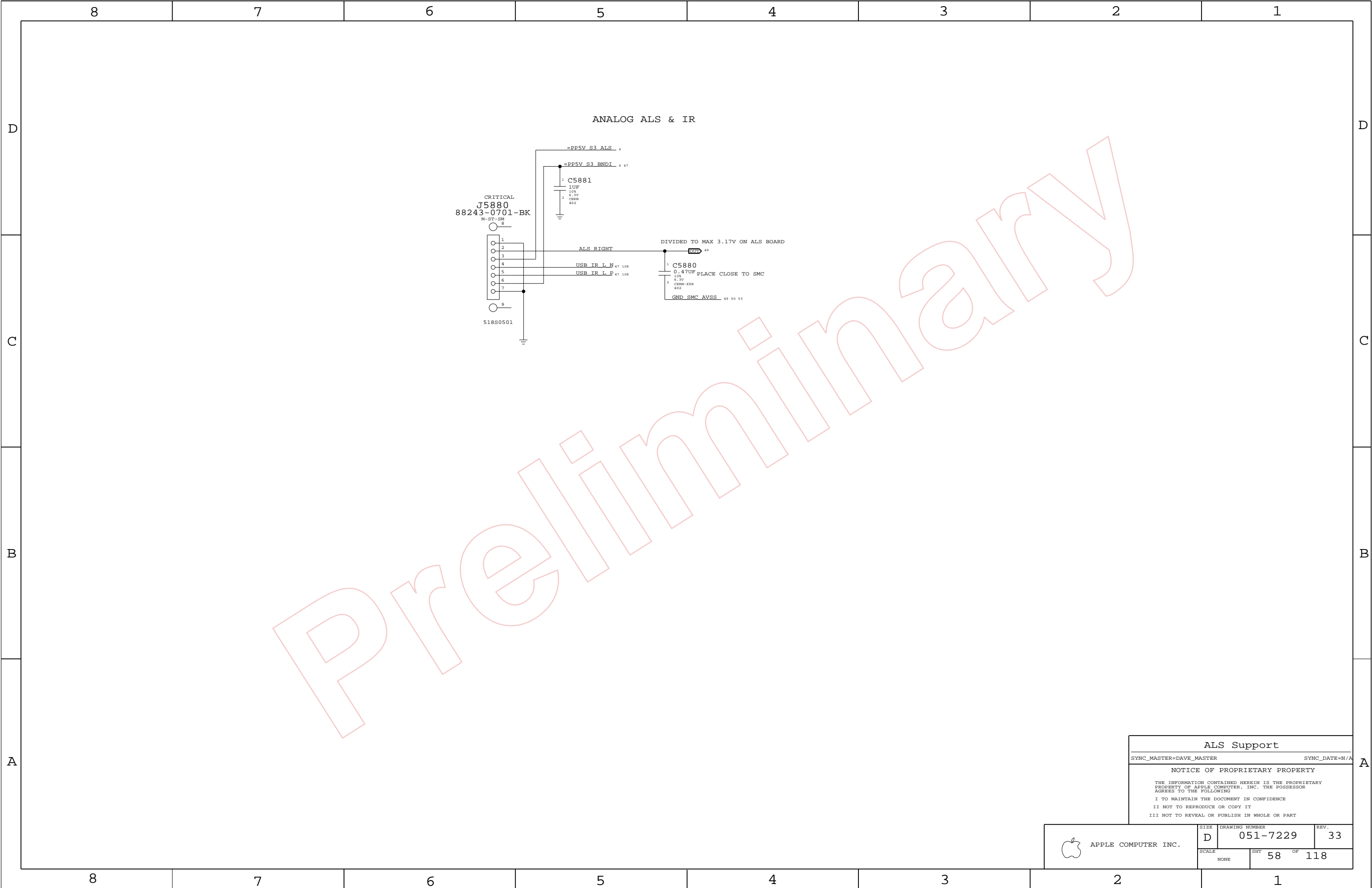
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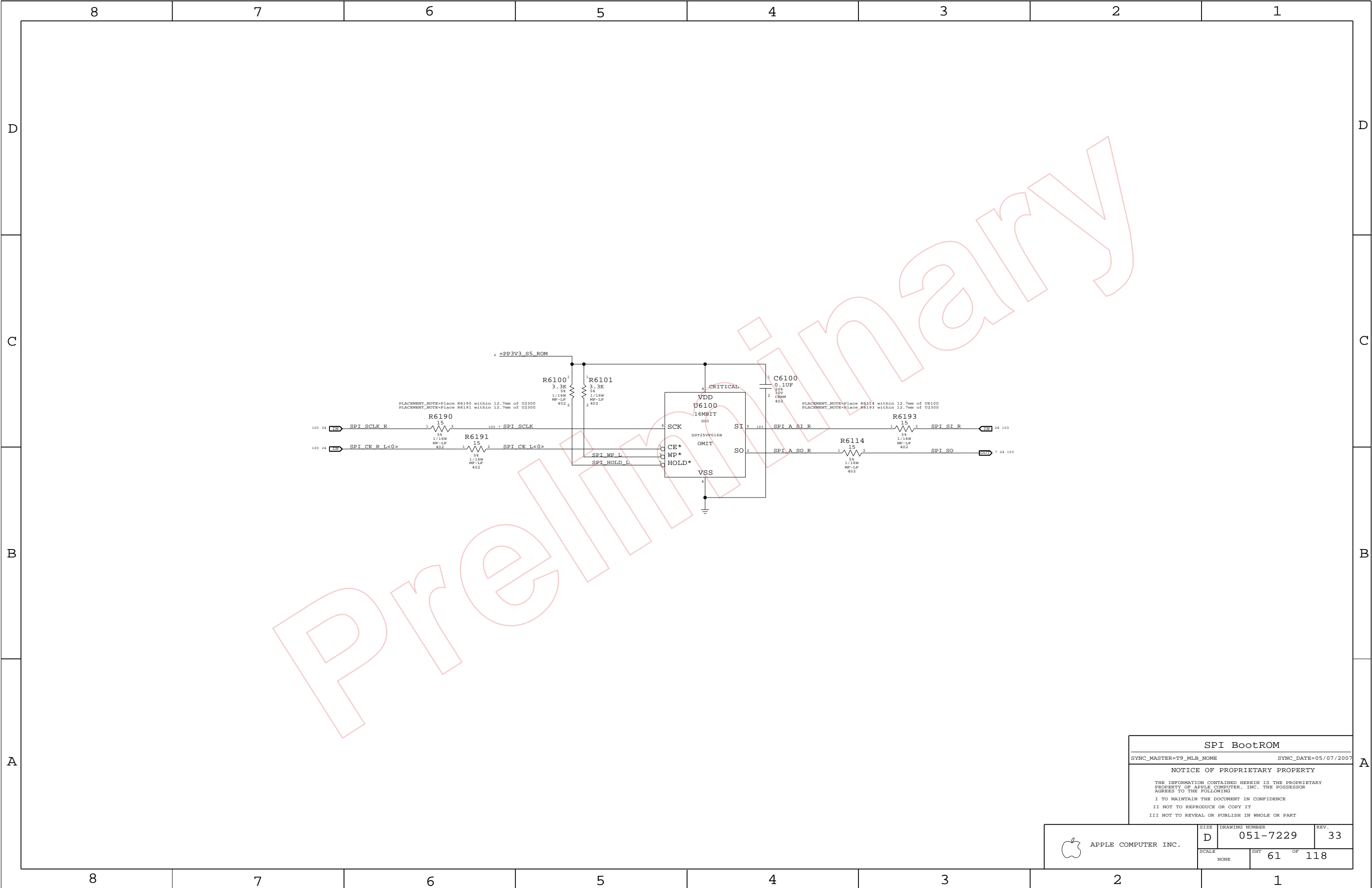
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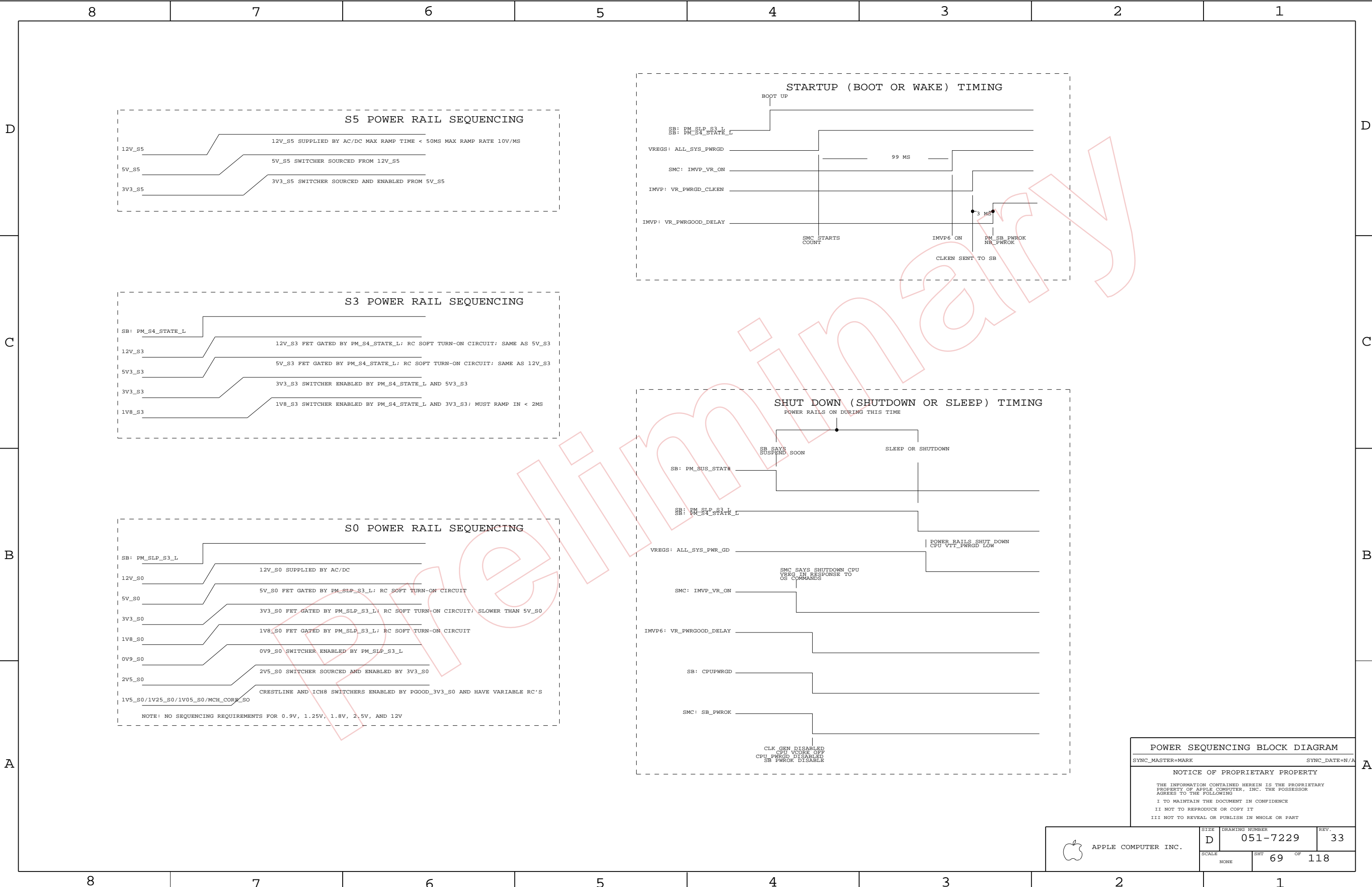
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7229	33
SCALE		SHT	OF
NONE		57	118







POWER SEQUENCING BLOCK DIAGRAM

SYNC_MASTER=MARK SYNC_DATE=N/A

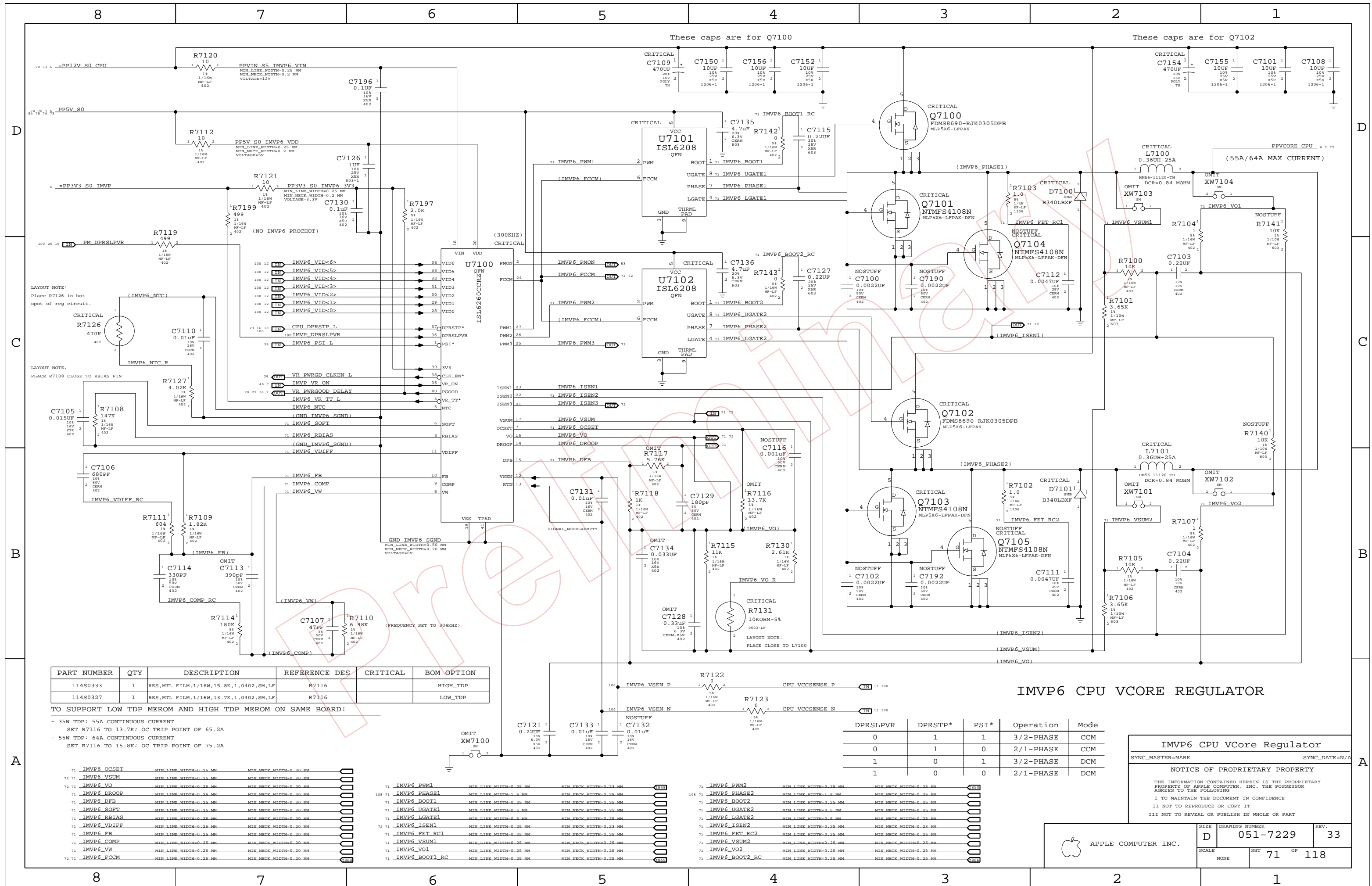
NOTICE OF PROPRIETARY PROPERTY

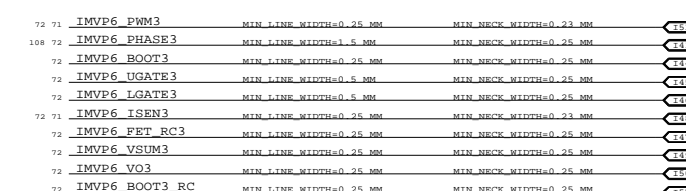
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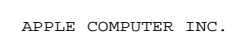
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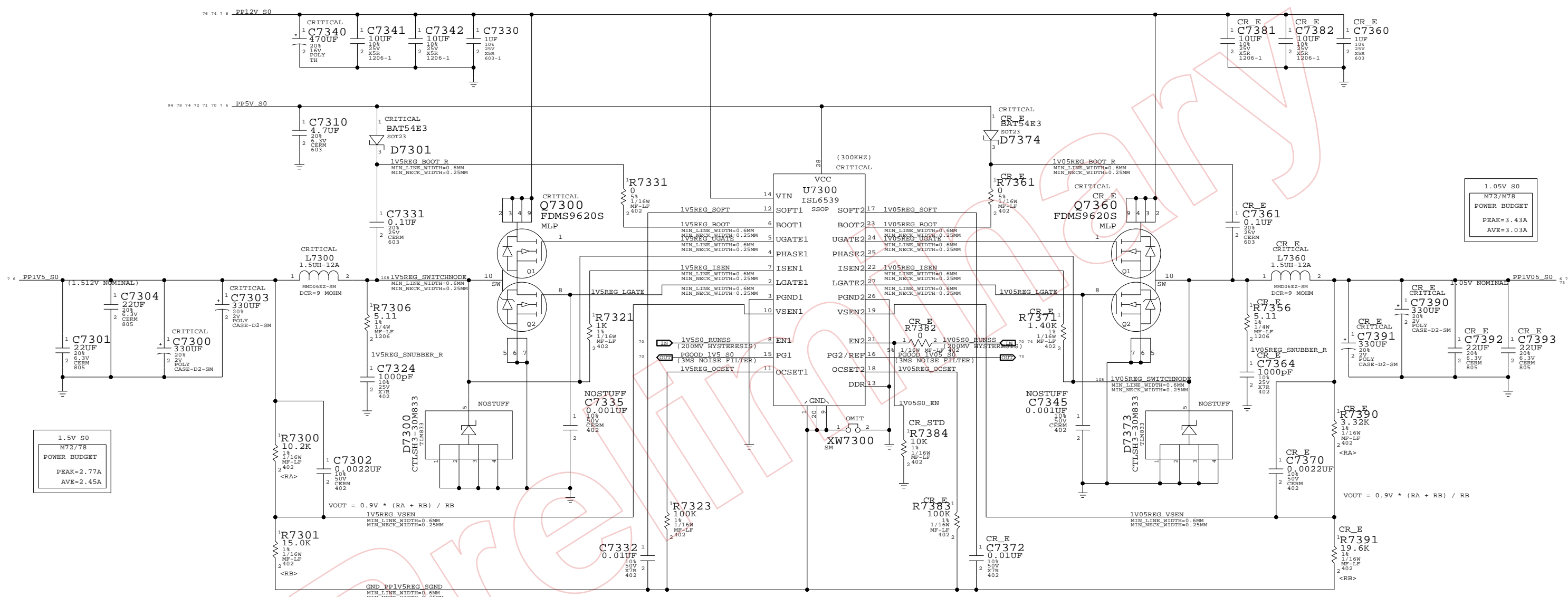




 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7229	REV. 33
	SCALE NONE	SHT 72	OF 118



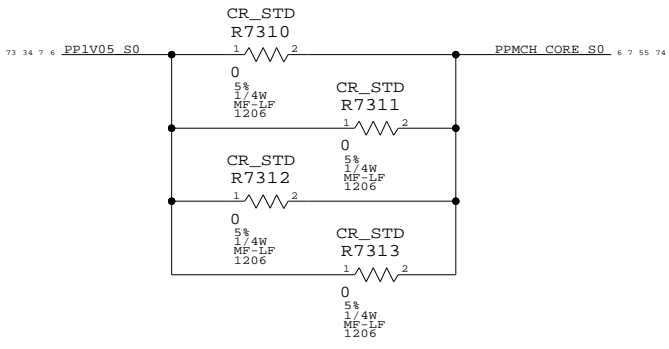
1.5V S0 & 1.05V SO RAILS



1.5V S0
M72/78
POWER BUDGET
PEAK=2.77A
AVE=2.45A

1.05V S0
M72/M78
POWER BUDGET
PEAK=3.43A
AVE=3.03A

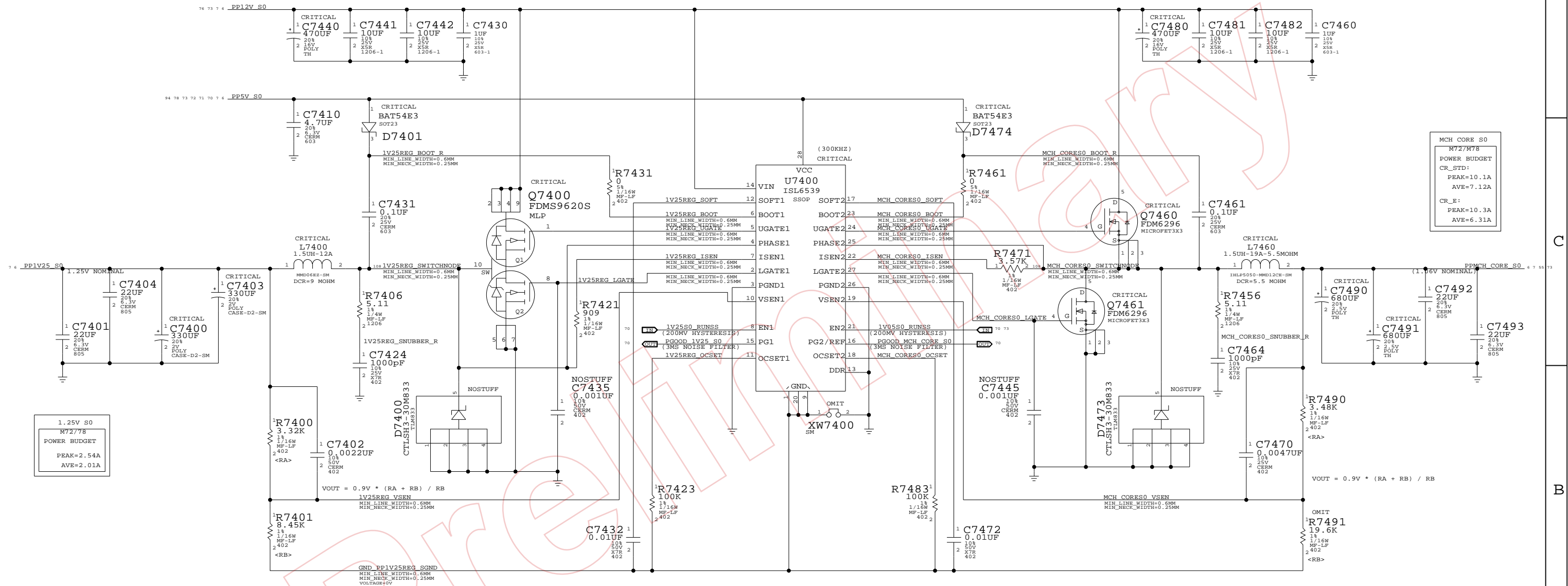
PLANE SHORTING RESISTORS



1.5V / 1.05V SUPPLIES
SYNC_MASTER=MARK SYNC_DATE=N/A
NOTICE OF PROPRIETARY PROPERTY
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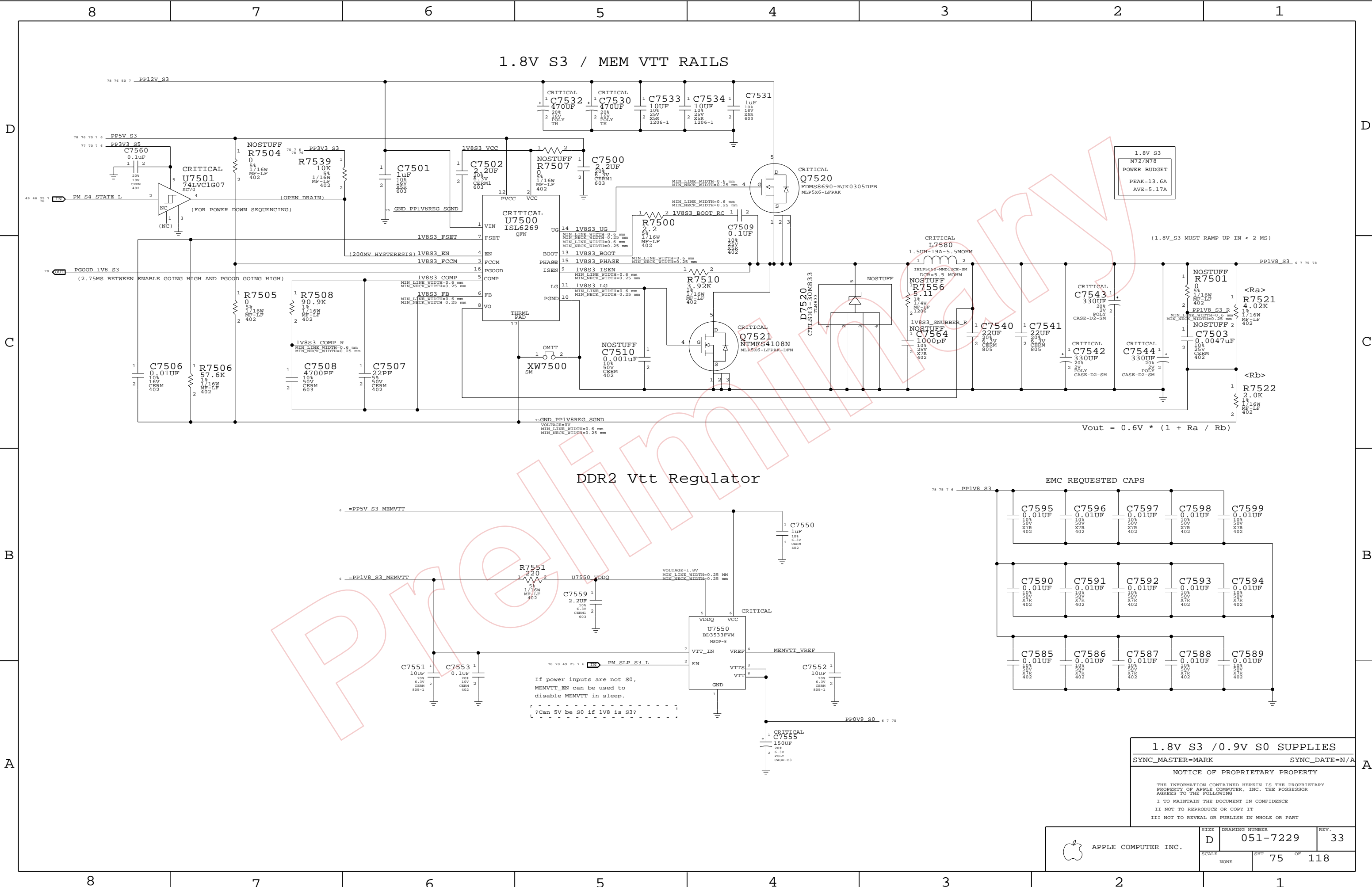
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7229	REV. 33
	SCALE NONE	SHT 73	OF 118

1.25V S0 & MCH CORE RAILS



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0342	1	RES,MTL FILM,1/16W,19.6K,1,0402,SMD,LF	R7491		CR_STD
114S0309	1	RES,MTL FILM,1/16W,8.66K,1,0402,SMD,LF	R7491		CR_E

1.25V / MCH CORE SUPPLIES	
SYNC_MASTER=MARK	SYNC_DATE=N/A
NOTICE OF PROPRIETARY PROPERTY	
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1.8V S3 / 0.9V S0 SUPPLIES
SYNC_MASTER=MARK SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

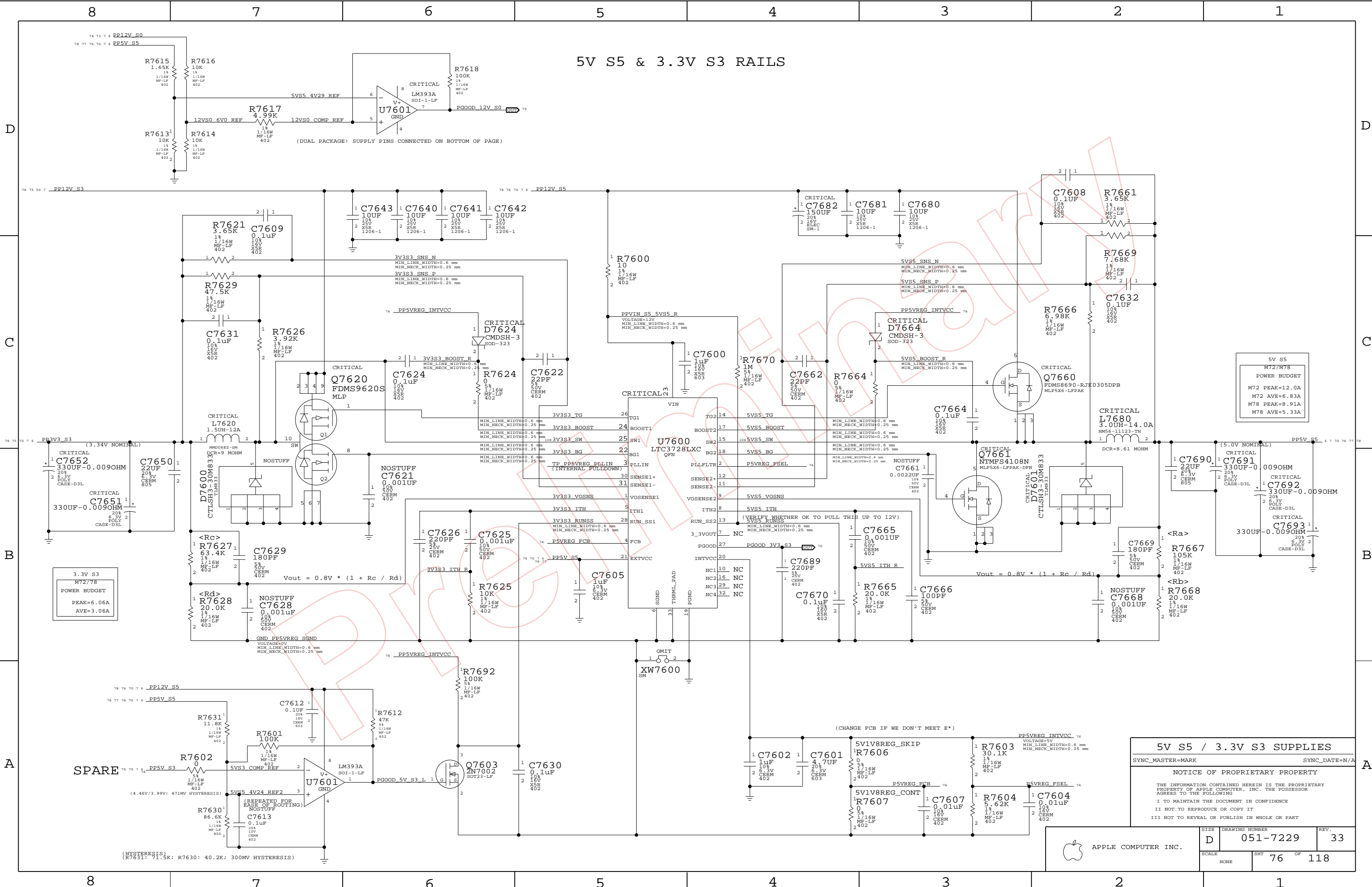
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7229	REV. 33
	SCALE NONE	SHT 75	OF 118



5V S5 & 3.3V S3 RAILS

5V S5
M72/M78
POWER BUDGET
M72 PEAK=12.0A
M72 AVE=6.83A
M78 PEAK=8.91A
M78 AVE=5.33A

3.3V S3
M72/M78
POWER BUDGET
PEAK=6.06A
AVE=3.06A

5V S5 / 3.3V S3 SUPPLIES		
SYNC_MASTER=MARK		SYNC_DATE=N/A
NOTICE OF PROPRIETARY PROPERTY		
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7229	REV. 33
	SCALE NONE	SHT 76	OF 118

D

C

B

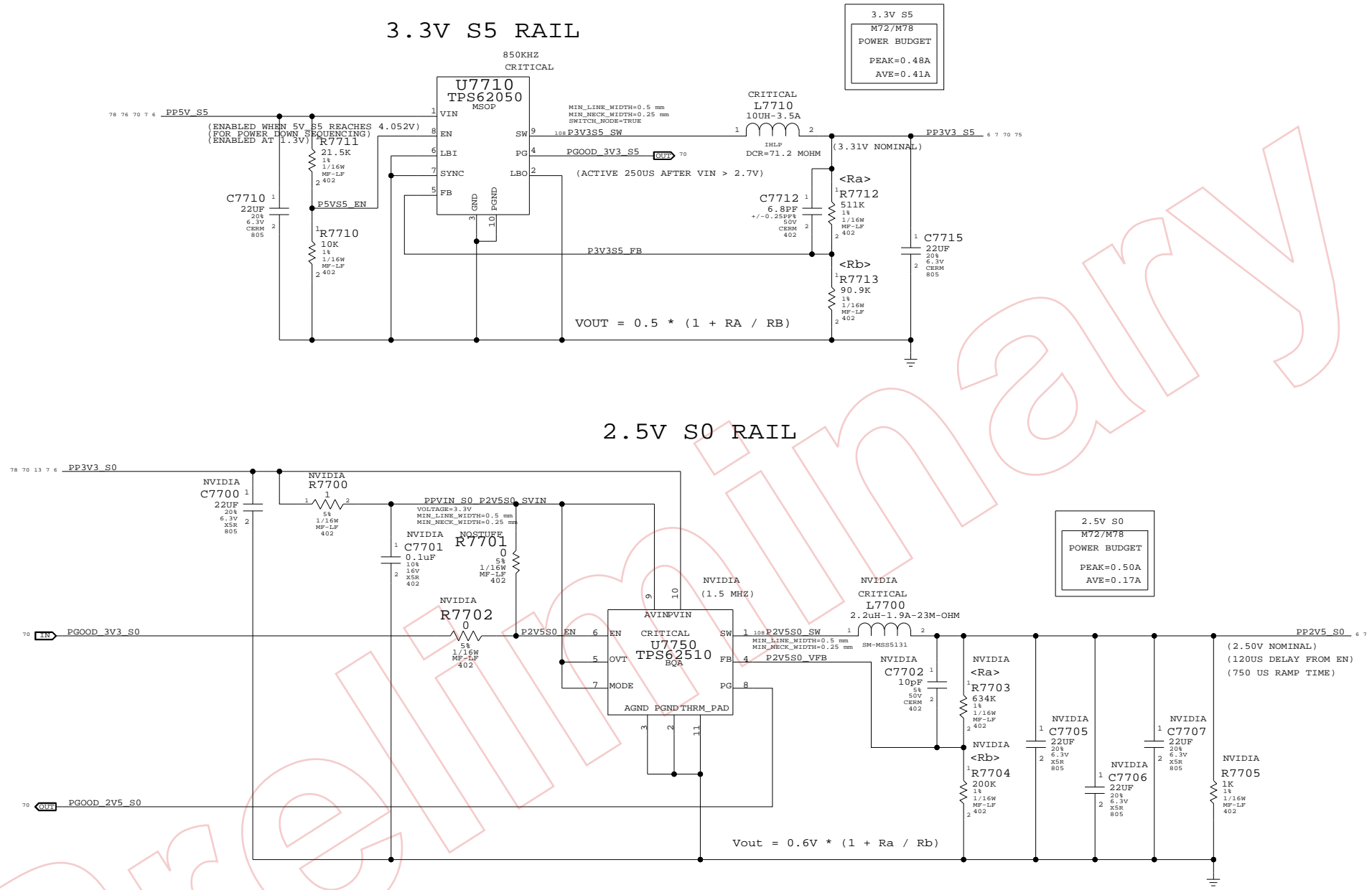
A

D

C

B

A



State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

3.3V / 2.5V POWER SUPPLIES

SYNC_MASTER=MARK

SYNC_DATE=N/A

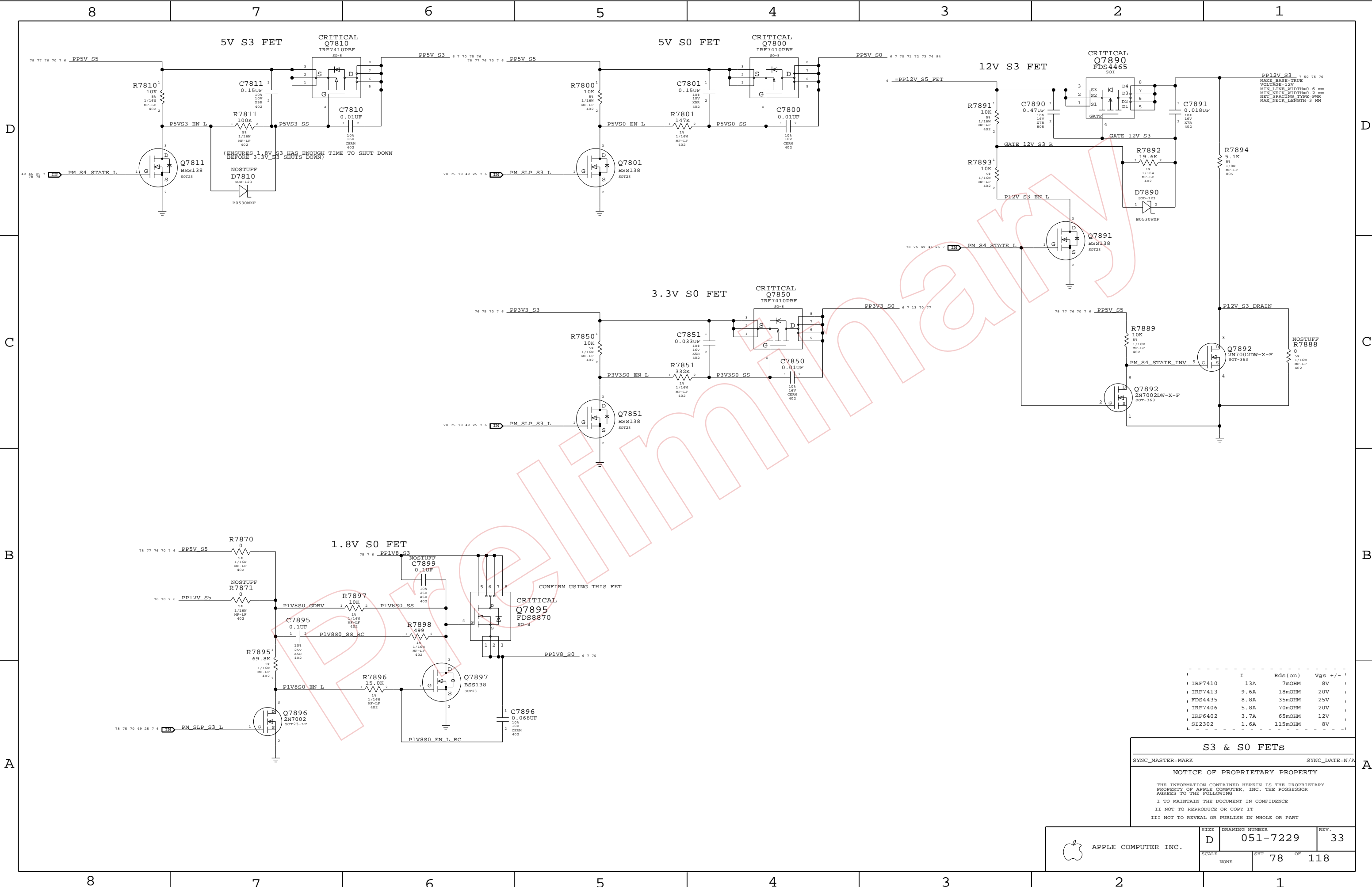
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	I	Rds (on)	Vgs +/-
IRF7410	13A	7mOHM	8V
IRF7413	9.6A	18mOHM	20V
FDS4435	8.8A	35mOHM	25V
IRF7406	5.8A	70mOHM	20V
IRF6402	3.7A	65mOHM	12V
SI2302	1.6A	115mOHM	8V

S3 & S0 FETs

SYNC_MASTER=MARK SYNC_DATE=N/A

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 APPLE COMPUTER INC.

SIZE D	DRAWING NUMBER 051-7229	REV. 33
SCALE NONE	SHT 78	OF 118

8

7

6

5

4

3

2

1

Page Notes

Power aliases required by this page:

- =PP12V_S0_MXM

- =PP5V_S0_MXM

- =PP1V8_S0_MXM

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

MXM SPEC POWER REQUIREMENTS

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE

CURRENT

POWER

3V3

1.5 A

4.95 W

5V

0.5 A

2.5 W

2V5

0.5 A

1.25 W

1V8

3.5 A

6.3 W

PWR (12V)

UP TO 4 A

PLATFORM DEPENDENT

Note: PCI-E Lanes are reversed to untangle routes

Need to stuff config strap using BOM option NBCFG_PEG_REVERSE

Polarity is also inverted (Tx+ goes to Rx-) to untangle routes

APPLE P/N: 516S0562

J8400

AS0B52X-S43E-XF

F-RT-SM

(1 OF 2)

CRITICAL

1V8RUN0

1V8RUN1

1V8RUN2

1V8RUN3

1V8RUN4

1V8RUN5

1V8RUN6

RUNPWROK

SVRUN

GND20

GND21

GND22

PWR_SRC0

PWR_SRC1

PWR_SRC2

PWR_SRC3

PWR_SRC4

PWR_SRC5

PWR_SRC6

PWR_SRC7

GND0

GND1

GND2

GND3

PPV_S0_MXM_PWRSRC

VOLTAGE=12V

MIN_LINE_WIDTH=0.150MM

MIN_SPACING=0.250MM

C8401

22UF

20V

5.3V

805

C8400

22UF

20V

35V

ELEC

SM-LF

70

50

49

7

ALL_SYS_PWRGD

PLACE CAPS NEAR NB

101 15

PEG R2D C P<0>

C8420

0.1uF

1

2

101 PEG R2D P<15>

40

PEX_TX15_L

37

PEG D2R N<0>

15

101

101 15

PEG R2D C N<0>

C8421

0.1uF

1

2

101 PEG R2D N<15>

42

PEX_TX15

39

PEG D2R P<0>

15

101

101 15

PEG R2D C P<1>

C8422

0.1uF

1

2

101 PEG R2D P<14>

44

PEX_TX14_L

43

PEG D2R N<1>

15

101

101 15

PEG R2D C N<1>

C8423

0.1uF

1

2

101 PEG R2D N<14>

46

PEX_TX14

45

PEG D2R P<1>

15

101

101 15

PEG R2D C P<2>

C8424

0.1uF

1

2

101 PEG R2D P<13>

48

PEX_TX13_L

47

PEG D2R N<2>

15

101

101 15

PEG R2D C N<2>

C8425

0.1uF

1

2

101 PEG R2D N<13>

50

PEX_TX13

49

PEG D2R P<2>

15

101

101 15

PEG R2D C P<3>

C8426

0.1uF

1

2

101 PEG R2D P<12>

52

PEX_TX12_L

51

PEG D2R N<3>

15

101

101 15

PEG R2D C N<3>

C8427

0.1uF

1

2

101 PEG R2D N<12>

54

PEX_TX12

53

PEG D2R P<3>

15

101

101 15

PEG R2D C P<4>

C8428

0.1uF

1

2

101 PEG R2D P<11>

56

PEX_TX11_L

55

PEG D2R N<4>

15

101

101 15

PEG R2D C N<4>

C8429

0.1uF

1

2

101 PEG R2D N<11>

58

PEX_TX11

57

PEG D2R P<4>

15

101

101 15

PEG R2D C P<5>

C8430

0.1uF

1

2

101 PEG R2D P<10>

60

PEX_TX10_L

59

PEG D2R N<5>

15

101

101 15

PEG R2D C N<5>

C8431

0.1uF

1

2

101 PEG R2D N<10>

62

PEX_TX10

61

PEG D2R P<5>

15

101

101 15

PEG R2D C P<6>

C8432

0.1uF

1

2

101 PEG R2D P<9>

64

PEX_TX9_L

63

PEG D2R N<6>

15

101

101 15

PEG R2D C N<6>

C8433

0.1uF

1

2

101 PEG R2D N<9>

66

PEX_TX9

65

PEG D2R P<6>

15

101

101 15

PEG R2D C P<7>

C8434

0.1uF

1

2

101 PEG R2D P<8>

68

PEX_TX8_L

67

PEG D2R N<7>

15

101

101 15

PEG R2D C N<7>

C8435

0.1uF

1

2

101 PEG R2D N<8>

70

PEX_TX8

69

PEG D2R P<7>

15

101

101 15

PEG R2D C P<8>

C8436

0.1uF

1

2

101 PEG R2D P<7>

72

PEX_TX7_L

71

PEG D2R N<8>

15

101

101 15

PEG R2D C N<8>

C8437

0.1uF

1

2

101 PEG R2D N<7>

74

PEX_TX7

73

PEG D2R P<8>

15

101

101 15

PEG R2D C P<9>

C8438

0.1uF

1

2

101 PEG R2D P<6>

76

PEX_TX6_L

75

PEG D2R N<9>

15

101

101 15

PEG R2D C N<9>

C8439

0.1uF

1

2

101 PEG R2D N<6>

78

PEX_TX6

77

PEG D2R P<9>

15

101

101 15

PEG R2D C P<10>

C8440

0.1uF

1

2

101 PEG R2D P<5>

80

PEX_TX5_L

79

PEG D2R N<10>

15

101

101 15

PEG R2D C N<10>

C8441

0.1uF

1

2

101 PEG R2D N<5>

82

PEX_TX5

81

PEG D2R P<10>

15

101

101 15

PEG R2D C P<11>

C8442

0.1uF

1

2

101 PEG R2D P<4>

84

PEX_TX4_L

83

PEG D2R N<11>

15

101

101 15

PEG R2D C N<11>

C8443

0.1uF

1

2

101 PEG R2D N<4>

<

```
- =PP12V_S0_MXM
- =PP5V_S0_MXM
- =PP1V8_S0_MXM
```

BOM options provided by this page:
(NONE)

8

7

6

5

4

3

2

1

Page Notes

Power aliases required by this page:

- =PP12V_S0_MXM

- =PP5V_S0_MXM

- =PP1V8_S0_MXM

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

MXM SPEC POWER REQUIREMENTS

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE

CURRENT

POWER

3V3

1.5 A

4.95 W

5V

0.5 A

2.5 W

2V5

0.5 A

1.25 W

1V8

3.5 A

6.3 W

PWR (12V)

UP TO 4 A

PLATFORM DEPENDENT

Note: PCI-E Lanes are reversed to untangle routes

Need to stuff config strap using BOM option NBCFG_PEG_REVERSE

Polarity is also inverted (Tx+ goes to Rx-) to untangle routes

APPLE P/N: 516S0562

J8400

AS0B52X-S43E-XF

F-RT-SM

(1 OF 2)

CRITICAL

1V8RUN0

1V8RUN1

1V8RUN2

1V8RUN3

1V8RUN4

1V8RUN5

1V8RUN6

RUNPWROK

SVRUN

GND20

GND21

GND22

PWR_SRC0

PWR_SRC1

PWR_SRC2

PWR_SRC3

PWR_SRC4

PWR_SRC5

PWR_SRC6

PWR_SRC7

GND0

GND1

GND2

GND3

PPV_S0_MXM_PWRSRC

VOLTAGE=12V

MIN_LINE_WIDTH=0.150MM

MIN_SPACING=0.250MM

C8401

22UF

20V

5.3V

805

C8400

22UF

20V

35V

ELEC

SM-LF

70

50

49

7

ALL_SYS_PWRGD

PRCNT2_L: RESERVED FOR FUTURE USE

KEY

PLACE CAPS NEAR NB

101 15

PEG_R2D_C_P<0>

C8420

0.1uF

1

2

101 PEG_R2D_P<15>

40

PEX_TX15_L

37

PEG_D2R_N<0>

15

101

101 15

PEG_R2D_C_N<0>

C8421

0.1uF

1

2

101 PEG_R2D_N<15>

42

PEX_TX15

39

PEG_D2R_P<0>

15

101

101 15

PEG_R2D_C_P<1>

C8422

0.1uF

1

2

101 PEG_R2D_P<14>

44

PEX_TX14_L

43

PEG_D2R_N<1>

15

101

101 15

PEG_R2D_C_N<1>

C8423

0.1uF

1

2

101 PEG_R2D_N<14>

46

PEX_TX14

45

PEG_D2R_P<1>

15

101

101 15

PEG_R2D_C_P<2>

C8424

0.1uF

1

2

101 PEG_R2D_P<13>

48

PEX_TX13_L

47

PEG_D2R_N<2>

15

101

101 15

PEG_R2D_C_N<2>

C8425

0.1uF

1

2

101 PEG_R2D_N<13>

50

PEX_TX13

49

PEG_D2R_P<2>

15

101

101 15

PEG_R2D_C_P<3>

C8426

0.1uF

1

2

101 PEG_R2D_P<12>

52

PEX_TX12_L

51

PEG_D2R_N<3>

15

101

101 15

PEG_R2D_C_N<3>

C8427

0.1uF

1

2

101 PEG_R2D_N<12>

54

PEX_TX12

53

PEG_D2R_P<3>

15

101

101 15

PEG_R2D_C_P<4>

C8428

0.1uF

1

2

101 PEG_R2D_P<11>

56

PEX_TX11_L

55

PEG_D2R_N<4>

15

101

101 15

PEG_R2D_C_N<4>

C8429

0.1uF

1

2

101 PEG_R2D_N<11>

58

PEX_TX11

57

PEG_D2R_P<4>

15

101

101 15

PEG_R2D_C_P<5>

C8430

0.1uF

1

2

101 PEG_R2D_P<10>

60

PEX_TX10_L

59

PEG_D2R_N<5>

15

101

101 15

PEG_R2D_C_N<5>

C8431

0.1uF

1

2

101 PEG_R2D_N<10>

62

PEX_TX10

61

PEG_D2R_P<5>

15

101

101 15

PEG_R2D_C_P<6>

C8432

0.1uF

1

2

101 PEG_R2D_P<9>

64

PEX_TX9_L

63

PEG_D2R_N<6>

15

101

101 15

PEG_R2D_C_N<6>

C8433

0.1uF

1

2

101 PEG_R2D_N<9>

66

PEX_TX9

65

PEG_D2R_P<6>

15

101

101 15

PEG_R2D_C_P<7>

C8434

0.1uF

1

2

101 PEG_R2D_P<8>

68

PEX_TX8_L

67

PEG_D2R_N<7>

15

101

101 15

PEG_R2D_C_N<7>

C8435

0.1uF

1

2

101 PEG_R2D_N<8>

70

PEX_TX8

69

PEG_D2R_P<7>

15

101

101 15

PEG_R2D_C_P<8>

C8436

0.1uF

1

2

101 PEG_R2D_P<7>

72

PEX_TX7_L

71

PEG_D2R_N<8>

15

101

101 15

PEG_R2D_C_N<8>

C8437

0.1uF

1

2

101 PEG_R2D_N<7>

74

PEX_TX7

73

PEG_D2R_P<8>

15

101

101 15

PEG_R2D_C_P<9>

C8438

0.1uF

1

2

101 PEG_R2D_P<6>

76

PEX_TX6_L

75

PEG_D2R_N<9>

15

101

101 15

PEG_R2D_C_N<9>

C8439

0.1uF

1

2

101 PEG_R2D_N<6>

78

PEX_TX6

77

PEG_D2R_P<9>

15

101

101 15

PEG_R2D_C_P<10>

C8440

0.1uF

1

2

101 PEG_R2D_P<5>

80

PEX_TX5_L

79

PEG_D2R_N<10>

15

101

101 15

PEG_R2D_C_N<10>

C8441

0.1uF

1

2

101 PEG_R2D_N<5>

82

PEX_TX5

81

PEG_D2R_P<10>

15

101

101 15

PEG_R2D_C_P<11>

C8442

0.1uF

1

2

101 PEG_R2D_P<4>

84

PEX_TX4_L

83

PEG_D2R_N<11>

15

101

101 15

PEG_R2D_C_N<11>

C8443

0.1uF

1

2

101 PEG_R2D_N<4>

86

PEX_TX4

85

PEG_D2R_P<11>

15

101

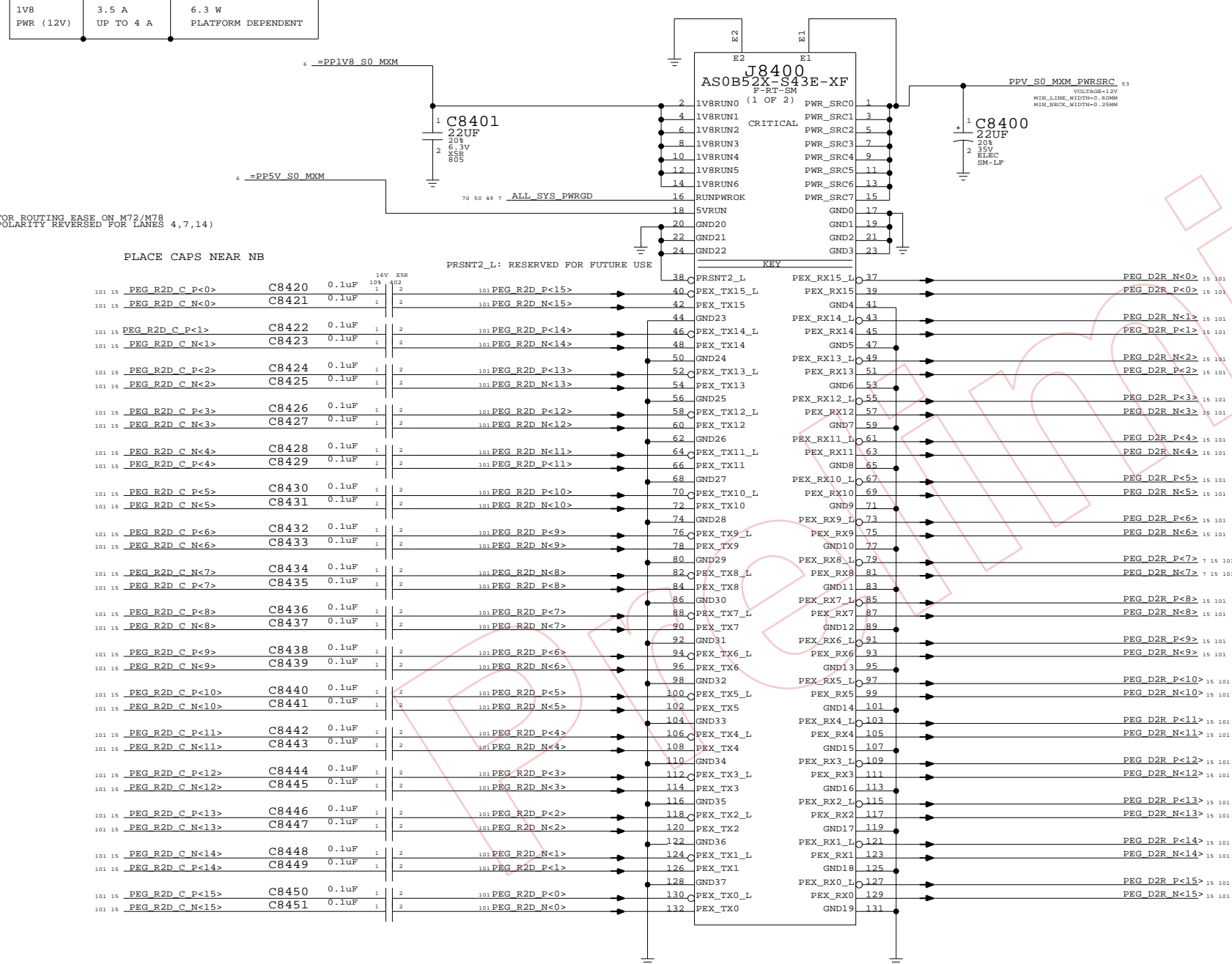
101 15

PEG_R2D_C_P<12>

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

APPLE P/N: 516S0562



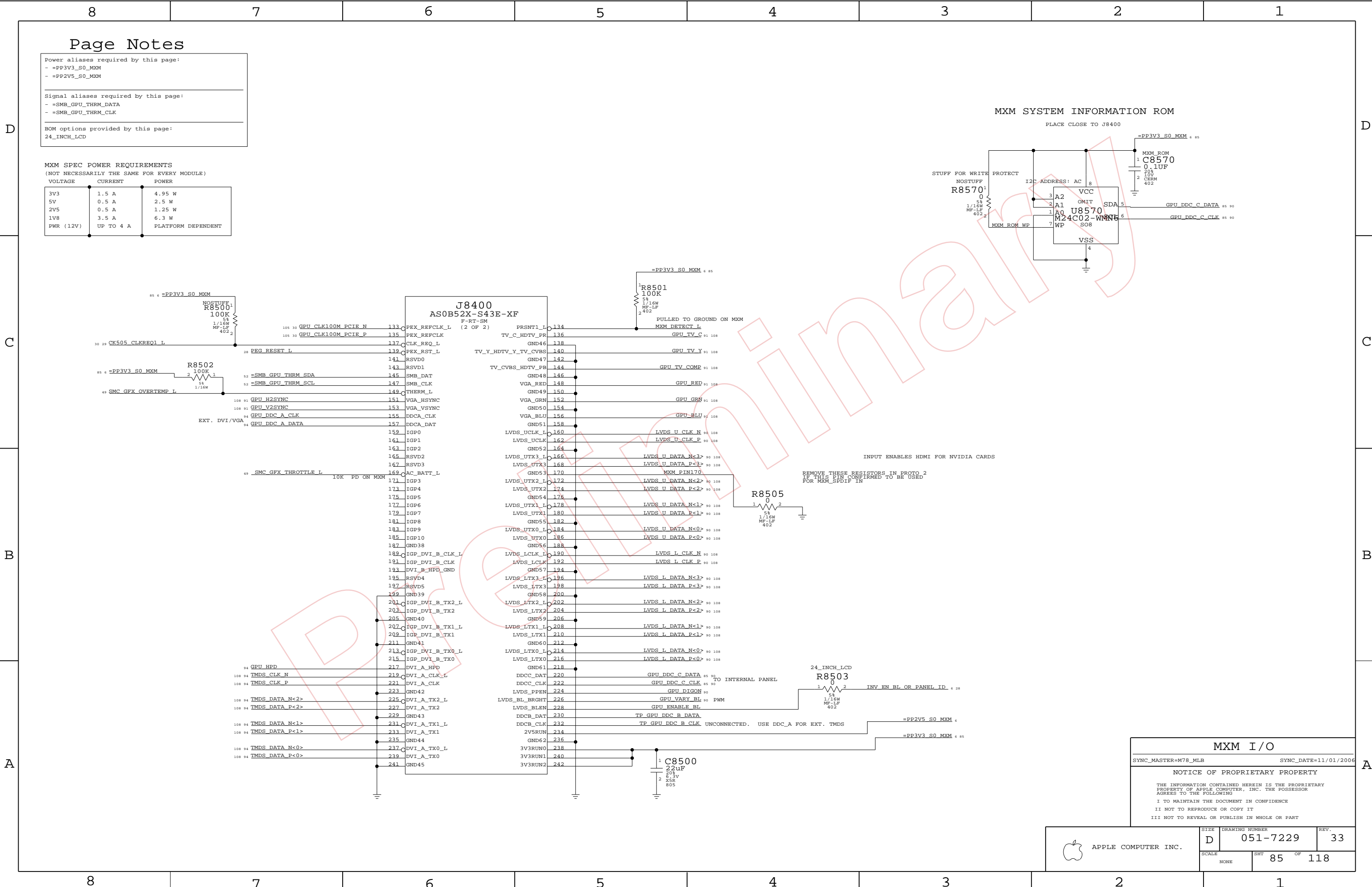
(FOR ROUTING EASE ON M72/M78
(POLARITY REVERSED FOR LANES 0-2)

MXM PCI-E & PWR	
SYNC_MASTER=M78_MLB	SYNC_DATE=11/01/2006
NOTICE OF PROPRIETARY PROPERTY	
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APPLE COMPUTER INC.

SIZE D	DRAWING NUMBER 051-7229	REV. 33
SCALE NONE	SHT 84	OF 118



Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP2V5_S0_MXM

Signal aliases required by this page:
- =SMB_GPU_THRM_DATA
- =SMB_GPU_THRM_CLK

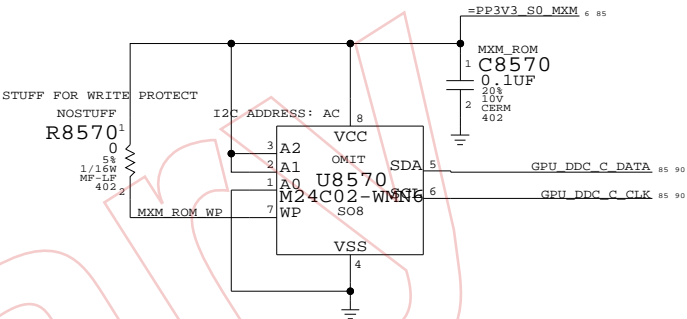
BOM options provided by this page:
24_INCH_LCD

MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400



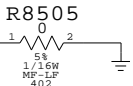
J8400
AS0B52X-S43E-XF

F-RT-SM
(2 OF 2)

133	PEX_REFCLK_L	134	PRSENT1_I
135	PEX_REFCLK	136	TV_C_HDTV_PR
137	CLK_REQ_L	138	GND46
139	PEX_RST_L	140	TV_Y_HDTV_Y_TV_CVBS
141	RSVD0	142	GND47
143	RSVD1	144	TV_CVBS_HDTV_PB
145	SMB_DAT	146	GND48
147	SMB_CLK	148	VGA_RED
149	THERM_L	150	GND49
151	VGA_HSYNC	152	VGA_GRN
153	VGA_VSYNC	154	GND50
155	DDCA_CLK	156	VGA_BLU
157	DDCA_DAT	158	GND51
159	IGP0	160	LVDS_U_CLK_N
161	IGP1	162	LVDS_U_CLK_P
163	IGP2	164	GND52
165	RSVD2	166	LVDS_UTX3_I
167	RSVD3	168	LVDS_UTX3_P
169	AC_BATT_L	170	GND53
171	IGP3	172	LVDS_UTX2_I
173	IGP4	174	LVDS_UTX2_P
175	IGP5	176	GND54
177	IGP6	178	LVDS_UTX1_I
179	IGP7	180	LVDS_UTX1_P
181	IGP8	182	GND55
183	IGP9	184	LVDS_UTX0_I
185	IGP10	186	LVDS_UTX0_P
187	GND38	188	GND56
189	IGP_DVI_B_CLK_L	190	LVDS_L_CLK_N
191	IGP_DVI_B_CLK	192	LVDS_L_CLK_P
193	DVI_B_HPD_GND	194	GND57
195	RSVD4	196	LVDS_L_TX3_I
197	RSVD5	198	LVDS_L_TX3_P
199	GND39	200	GND58
201	IGP_DVI_B_TX2_L	202	LVDS_L_TX2_I
203	IGP_DVI_B_TX2	204	LVDS_L_TX2_P
205	GND40	206	GND59
207	IGP_DVI_B_TX1_L	208	LVDS_L_TX1_I
209	IGP_DVI_B_TX1	210	LVDS_L_TX1_P
211	GND41	212	GND60
213	IGP_DVI_B_TX0_L	214	LVDS_L_TX0_I
215	IGP_DVI_B_TX0	216	LVDS_L_TX0_P
217	DVI_A_HPD	218	GND61
219	DVI_A_CLK_L	220	DDCC_DAT
221	DVI_A_CLK	222	DDCC_CLK
223	GND42	224	LVDS_PPEN
225	DVI_A_TX2_L	226	LVDS_BL_BRGHT
227	DVI_A_TX2	228	LVDS_BLEN
229	GND43	230	DDCB_DAT
231	DVI_A_TX1_L	232	DDCB_CLK
233	DVI_A_TX1	234	2V5RUN
235	GND44	236	GND62
237	DVI_A_TX0_L	238	3V3RUN0
239	DVI_A_TX0	240	3V3RUN1
241	GND45	242	3V3RUN2

INPUT ENABLES HDMI FOR NVIDIA CARDS

REMOVE THESE RESISTORS IN PROTO 2
IF THIS PIN CONFIRMED TO BE USED
FOR MXM_SPDIF IN



24_INCH_LCD



MXM I/O

SYNC_MASTER=M78_MLB SYNC_DATE=11/01/2006

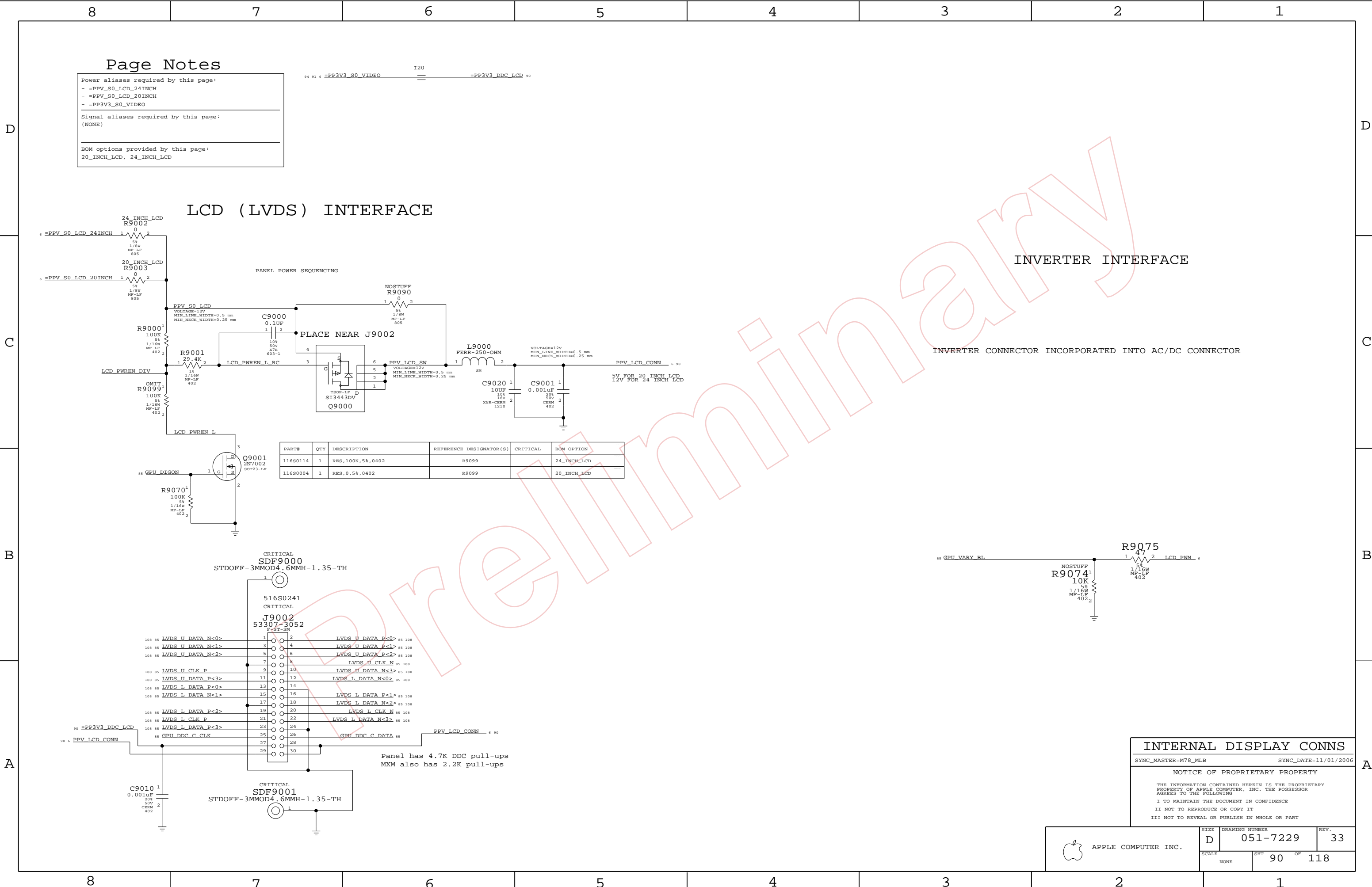
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SCALE	SHT	OF
NONE	85	118



INTERNAL DISPLAY CONNS

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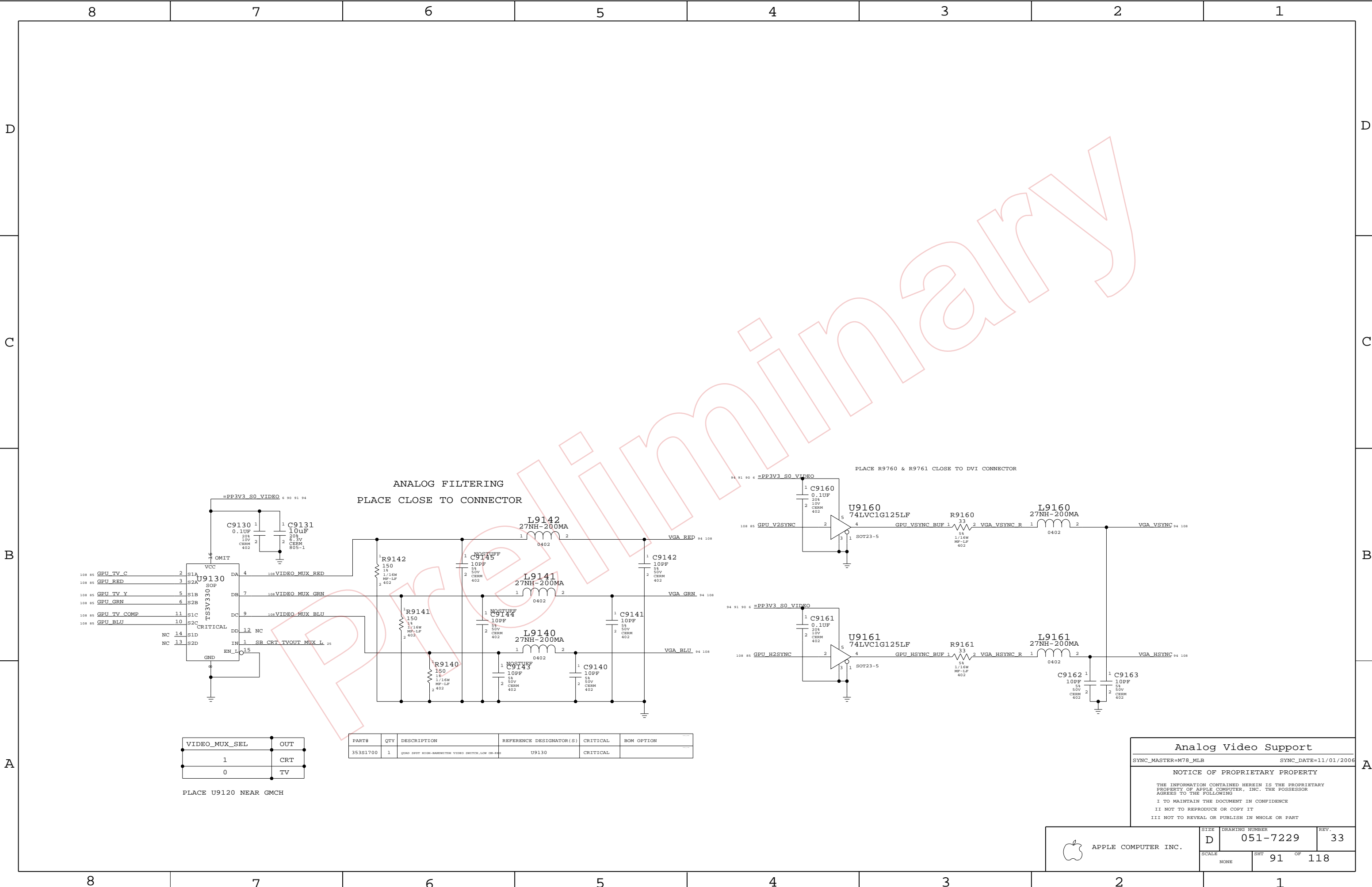
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Analogue Video Support

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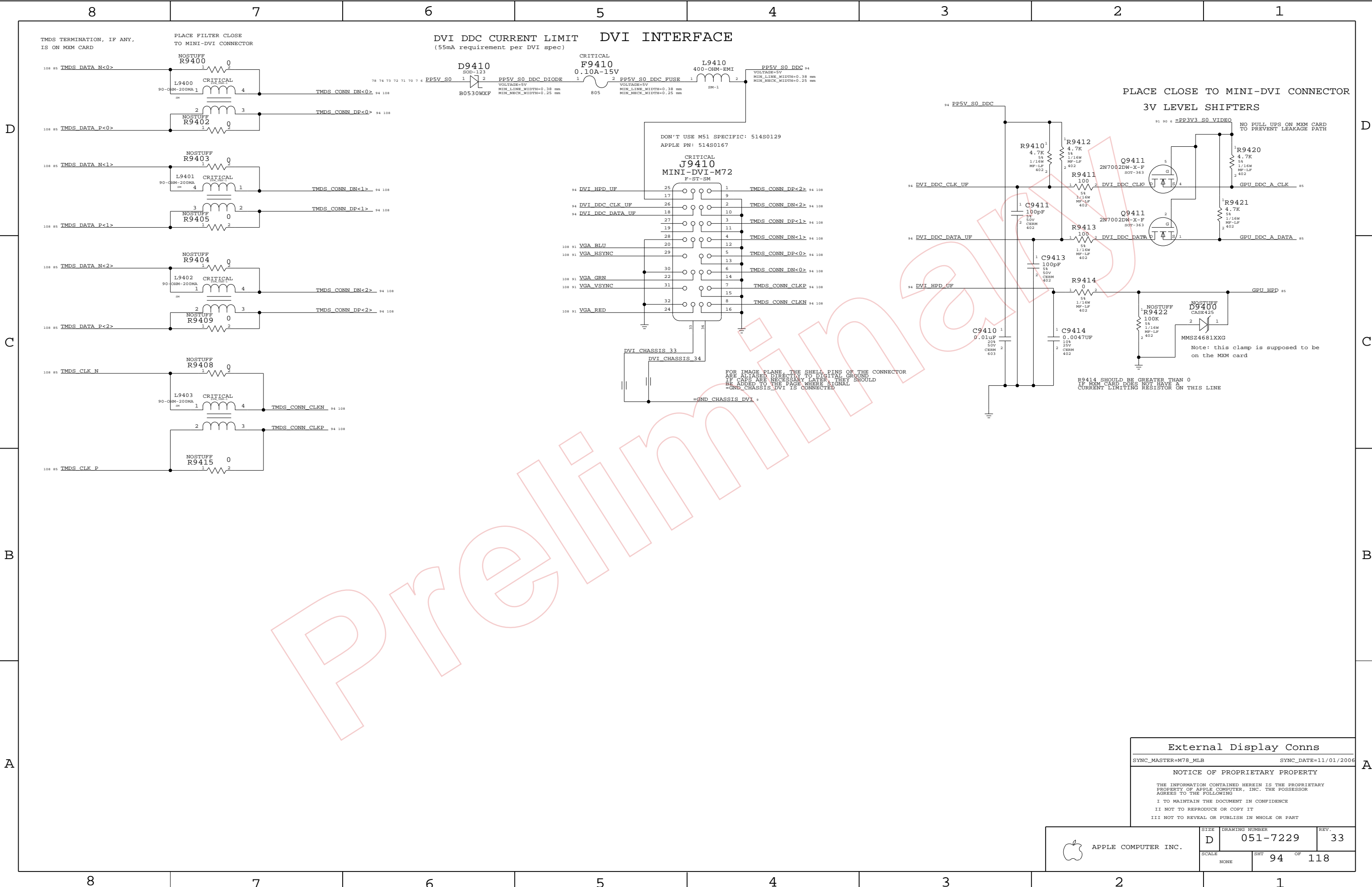
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External Display Conns

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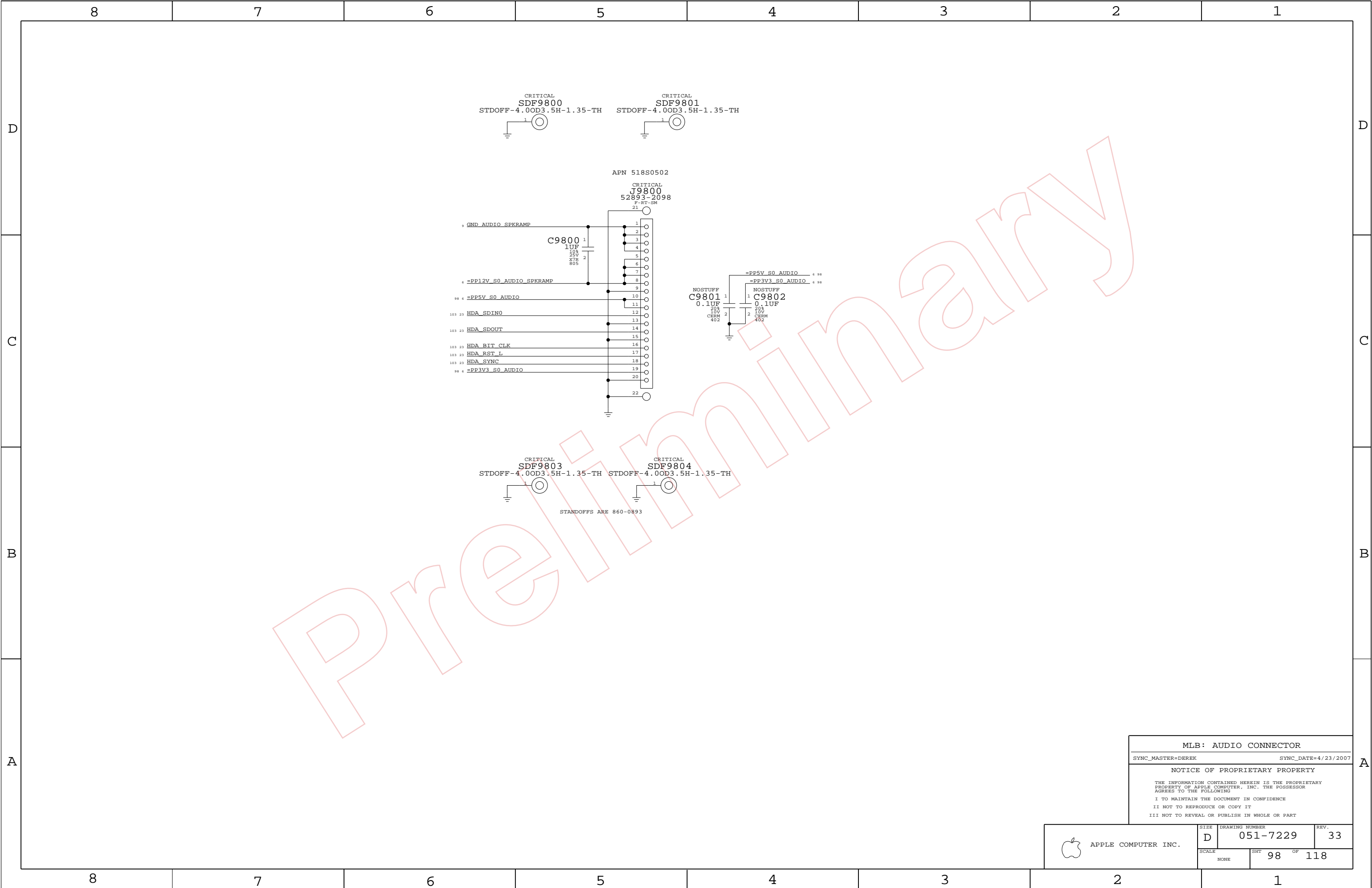
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SCALE		SHT	OF
NONE		94	118



Disk Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
IDE_55S	*	55_OHM_SE
SATA_55S	*	55_OHM_SE
SATA_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
IDE	*	*	SPACING_0.18MM
SATA	*	*	SPACING_0.5MM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HDA_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDA	*	*	SPACING_0.18MM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_60S	*	55_OHM_SE
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	SPACING_0.5MM

DG SAYS MINIMUM SPACING 50 MILS FROM USB TO CLOCKS

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_55S	*	55_OHM_SE
SPI_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SPACING_0.3MM
SPI	*	*	SPACING_0.18M

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	IDE_PDD	IDE 558	IDE	IDE PDD<15...10>	23 44
	IDE_PDD_PP	IDE 558	IDE	IDE PDD<9>	7 23 44
	IDE_PDD	IDE 558	IDE	IDE PDD<8...0>	23 44
	IDE_PDA	IDE 558	IDE	IDE PDA<2...0>	23 44
	IDE_PDCS	IDE 558	IDE	IDE PDCS1 L	23 44
	IDE_PDCS	IDE 558	IDE	IDE PDCS3 L	23 44
	IDE_PDIOW	IDE 558	IDE	IDE PDIOW L	23 44
	IDE_PDIOR L	IDE 558	IDE	IDE PDIOR L	7 23 44
	IDE_PDDACK L	IDE 558	IDE	IDE PDDACK L	23 44
	IDE_PDDREQ	IDE 558	IDE	IDE PDDREQ	23 44
	IDE_PDIORDY	IDE 558	IDE	IDE PDIORDY	7 23 44
	IDE_IRQ14	IDE 558	IDE	IDE IRQ14	23 44
	IDE_RST L	IDE 558	IDE	ODD_RST 5VTOL L	24 44
	SATA_A_R2D	SATA 100D	SATA	SATA A_R2D C_P	23 44
		SATA 100D	SATA	SATA A_R2D C_N	23 44
		SATA 100D	SATA	SATA A_R2D P	45
		SATA 100D	SATA	SATA A_R2D N	45
	SATA_A_D2R	SATA 100D	SATA	SATA A_D2R P	7 23 45
		SATA 100D	SATA	SATA A_D2R N	7 23 45
		SATA 100D	SATA	SATA A_D2R C_P	45
		SATA 100D	SATA	SATA A_D2R C_N	45
		SATA 100D	SATA	SATA B_R2D C_P	23 45
		SATA 100D	SATA	SATA B_R2D C_N	23 45
		SATA 100D	SATA	SATA_B_D2R P	23 45
		SATA 100D	SATA	SATA_B_D2R N	23 45
	SATA_RBIAS	SATA 558		SATA RBIAS	45
	HDA_BIT_CLK	HDA 558	HDA	HDA_BIT_CLK	23 98
		HDA 558	HDA	HDA_BIT_CLK_R	23
	HDA_SYNC	HDA 558	HDA	HDA_SYNC	23 98
		HDA 558	HDA	HDA_SYNC_R	23
	HDA_RST L	HDA 558	HDA	HDA_RST L	23 98
		HDA 558	HDA	HDA_RST L_R	23
	HDA_SDIN0	HDA 558	HDA	HDA_SDIN0	23 98
		HDA 558	HDA	HDA_SDIN CODEC	
	HDA_SDOUT	HDA 558	HDA	HDA_SDOUT	23 98
		HDA 558	HDA	HDA_SDOUT_R	23
	USB_EXTN	USB 90D	USB	USB_EXTN P	24 46
		USB 90D	USB	USB_EXTN N	24 46
		USB 90D	USB	USB_EXTN MIXED P	
		USB 90D	USB	USB_EXTN MIXED N	
	USB_MINI	USB 90D	USB	USB_MINI P	24 34
		USB 90D	USB	USB_MINI N	24 34
		USB 90D	USB	USB_EXTD P	24 46
		USB 90D	USB	USB_EXTD N	24 46
	USB_CAMERA	USB 90D	USB	USB_CAMERA P	7 24 47
		USB 90D	USB	USB_CAMERA N	7 24 47
	USB_BT	USB 90D	USB	USB_BT P	7 24 47
		USB 90D	USB	USB_BT N	7 24 47
		USB 90D	USB	USB_TPAD P	24 47
		USB 90D	USB	USB_TPAD N	24 47
	USB_IR	USB 90D	USB	USB_IR P	7 24 47
		USB 90D	USB	USB_IR N	24 47
	USB_EXTR	USB 90D	USB	USB_EXTR P	24 46
		USB 90D	USB	USB_EXTR N	24 46
		USB 90D	USB	USB_EXCARD P	24 47
		USB 90D	USB	USB_EXCARD N	24 47
	USB_EXTC	USB 90D	USB	USB_EXTC P	24 46
		USB 90D	USB	USB_EXTC N	24 46
	USB_RBIAS	USB 60S		USB RBIAS	24
	SMB_SR_SCL	SMB 558	SMB	SMB_CLK	25 52
	SMB_SR_SDA	SMB 558	SMB	SMB_DATA	25 52
	SMB_SR_MR_SCL	SMB 558	SMB	SMB_ME_CLK	25 52
	SMB_SR_MR_SDA	SMB 558	SMB	SMB_ME_DATA	25 52
	SPI_SCLK	SPI 558	SPI	SPI_SCLK R	24 61
		SPI 558	SPI	SPI_SCLK	7 61
		SPI 558	SPI	SPI_A_SCLK R	
		SPI 558	SPI	SPI_B_SCLK R	
	SPI_SI	SPI 558	SPI	SPI_SI R	24 61
		SPI 558	SPI	SPI_SI	
		SPI 558	SPI	SPI_A_SI R	61
		SPI 558	SPI	SPI_B_SI R	
	SPI_SO	SPI 558	SPI	SPI_SO	7 24 61
		SPI 558	SPI	SPI_A_SO R	7 61
		SPI 558	SPI	SPI_B_SO	
		SPI 558	SPI	SPI_B_SO R	
	SPI_CE L<0>	SPI 558	SPI	SPI_CE R L<0>	24 61
		SPI 558	SPI	SPI_CE L<0>	7 61
	SPI_CE L<1>	SPI 558	SPI	SPI_CE R L<1>	
		SPI 558	SPI	SPI_CE L<1>	

SB Constraints (1 of 2)

SYNC_MASTER=T9_MLB	SYNC_DATE=09/27/2006
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SCALE NONE	SHT 103	OF 118

PCI Bus Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCI_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	*	*	STANDARD

CHANGED TO 0.1MM SPACING AS THERE ARE NO PCI DEVICES

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLINK_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK	*	*	SPACING_0.18MM
CLINK_VREF	*	*	SPACING_0.3MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_12MIL	*	=STANDARD	0.3 MM	0.125 MM	7.5 MM	=STANDARD	=STANDARD

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	*	*	SPACING_0.5MM
ENET_MDI	ENET_MDI_TERM	*	SPACING_0.2MM

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
		PCT_55S	PCT	PCI AD<18..0>
		PCT_55S	PCT	PCI AD<19>
		PCT_55S	PCT	PCI AD<20>
		PCT_55S	PCT	PCI AD<31..21>
		PCT_55S	PCT	PCI PAR
		PCT_55S	PCT	PCI C BE L<3..0>
		PCT_55S	PCT	PCI IRDY L
		PCT_55S	PCT	PCI DEVSEL L
		PCT_55S	PCT	PCI PERR L
		PCT_55S	PCT	PCI LOCK L
		PCT_55S	PCT	PCI SERR L
		PCT_55S	PCT	PCI STOP L
		PCT_55S	PCT	PCI TRDY L
		PCT_55S	PCT	PCI FRAME L
		PCT_55S	PCT	PCI FW REQ L
		PCT_55S	PCT	PCI FW GNT L
		PCT_55S	PCT	PCI REQ1 L
		PCT_55S	PCT	PCI GNT1 L
		PCT_55S	PCT	PCI REQ2 L
		PCT_55S	PCT	PCI GNT2 L
	INT_PIRQA_L	PCT_55S	PCT	INT_PIRQA_L
	INT_PIRQB_L	PCT_55S	PCT	INT_PIRQB_L
	INT_PIROC_L	PCT_55S	PCT	INT_PIROC_L
	INT_PIROD_L	PCT_55S	PCT	INT_PIROD_L
	INT_PIROE_L	PCT_55S	PCT	INT_PIROE_L
	INT_PIROF_L	PCT_55S	PCT	INT_PIROF_L
	PCIE_A_R2D	PCIE_100D	PCIE	PCIE MINI R2D C P
		PCIE_100D	PCIE	PCIE MINI R2D C N
	PCIE_A_D2R	PCIE_100D	PCIE	PCIE MINI D2R P
		PCIE_100D	PCIE	PCIE MINI D2R N
	PCIE_B_R2D	PCIE_100D	PCIE	PCIE ENET R2D C P
		PCIE_100D	PCIE	PCIE ENET R2D C N
	PCIE_B_D2R	PCIE_100D	PCIE	PCIE ENET D2R P
		PCIE_100D	PCIE	PCIE ENET D2R N
	PCIE_C_R2D	PCIE_100D	PCIE	PCIE FW R2D C P
		PCIE_100D	PCIE	PCIE FW R2D C N
	PCIE_B_D2R	PCIE_100D	PCIE	PCIE FW D2R P
		PCIE_100D	PCIE	PCIE FW D2R N
	GLAN_COMP			GLAN COMP
	CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK
	CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA
	CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L
	NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB CLINK VREF
	SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB CLINK VREF0
	SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB CLINK VREF1
ENET			ENET	PPIV9R2V5 S3 ENET PHY AVDD
ENET			ENET	PPIV9R2V5 S3 ENET R
MDIO			ENET MDI_TERM	ENET MDIO
MDIO			ENET MDI_TERM	ENET MDI1
MDIO			ENET MDI_TERM	ENET MDI2
MDIO			ENET MDI_TERM	ENET MDI3
ENET MDIO	ENET MDIO	ENET_100D	ENET MDI	ENET MDI P<0>
ENET MDI1	ENET MDI1	ENET_100D	ENET MDI	ENET MDI N<0>
ENET MDI2	ENET MDI2	ENET_100D	ENET MDI	ENET MDI P<1>
ENET MDI3	ENET MDI3	ENET_100D	ENET MDI	ENET MDI N<1>
ENET MDI2	ENET MDI2	ENET_100D	ENET MDI	ENET MDI P<2>
ENET MDI3	ENET MDI3	ENET_100D	ENET MDI	ENET MDI N<2>
ENET MDI3	ENET MDI3	ENET_100D	ENET MDI	ENET MDI P<3>
ENET MDI3	ENET MDI3	ENET_100D	ENET MDI	ENET MDI N<3>

SB Constraints (2 of 2)

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SYNC_MASTER=(MASTER)
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SYNC_DATE=(10/02/2006)

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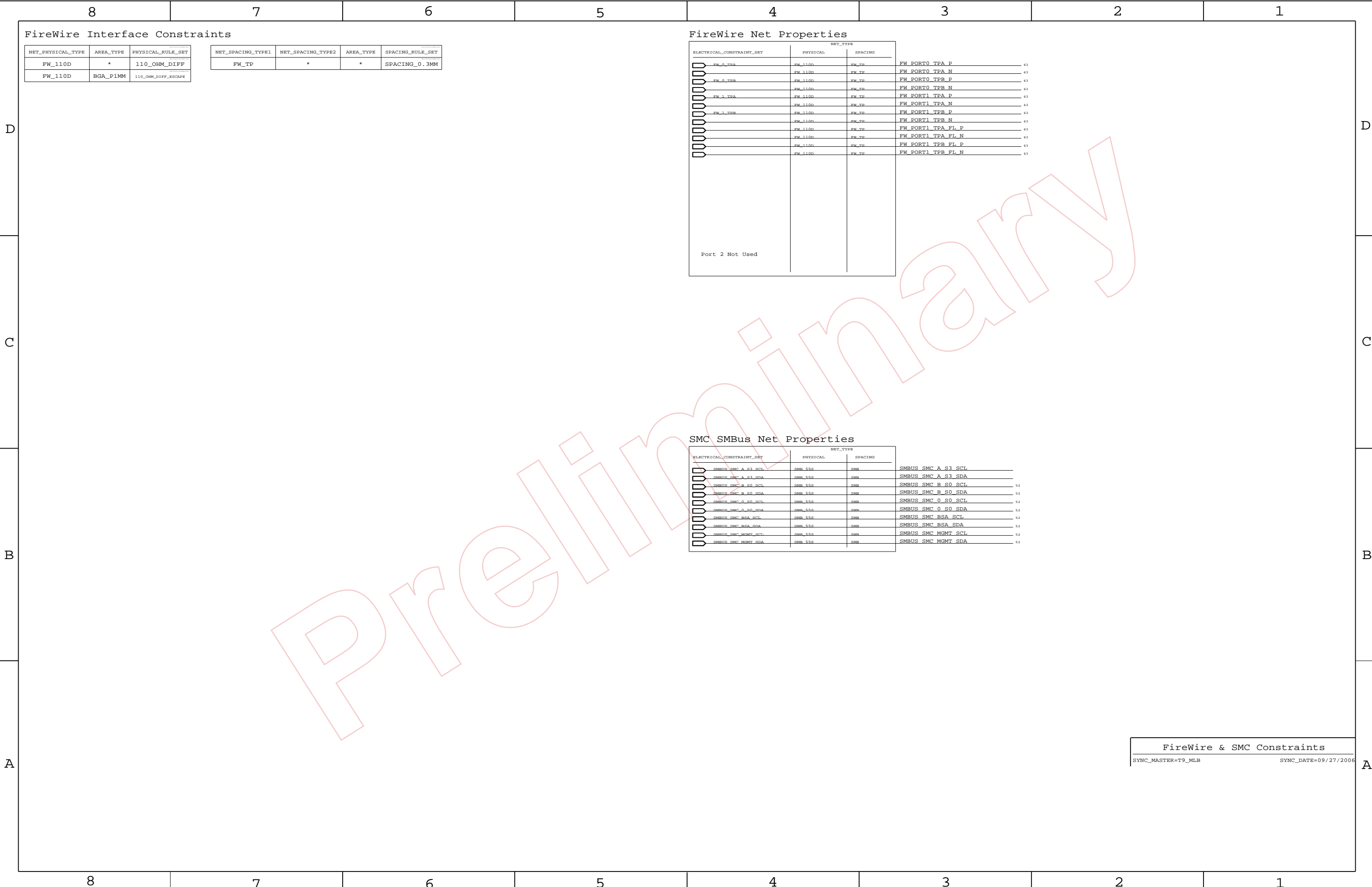
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1

8			7			6			5			4			3			2			1					
Clock Signal Constraints																										
NET_PHYSICAL_TYPE			AREA_TYPE			PHYSICAL_RULE_SET			NET_SPACING_TYPE1			NET_SPACING_TYPE2			AREA_TYPE			SPACING_RULE_SET								
CLK_FSB_100D			*			100_OHM_DIFF			CLK_FSB			*			*			CLK_SPACING_0.6MM								
CLK_PCIE_100D			*			100_OHM_DIFF			CLK_PCIE			*			*			CLK_SPACING_0.5MM								
CLK_MED_55S			*			55_OHM_SE			CLK_MED			*			*			CLK_SPACING_0.5MM								
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6																										
Clock Net Properties																										
ELECTRICAL_CONSTRAINT_SET																										
NET_TYPE																										
PHYSICAL																										
SPACING																										
CK505_CPU																										
CK505_CPU																										
CK505_NB																										
CK505_NB																										
CK505_ITP																										
CK505_ITP																										
CK505_PCIF0																										
CK505_PCIF1																										
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<table><tr><th rowspan="2">ELECTRICAL_CONSTRAINT_SET</th><th colspan="2">NET_TYPE</th><th rowspan="2"></th><th rowspan="2"></th></tr><tr><th>PHYSICAL</th><th>SPACING</th></tr><tr><td>TMDS_DATA</td><td>TMDS_100n</td><td>TMDS</td><td>TMDS DATA P<3..0></td><td>85 94</td></tr><tr><td>TMDS_100n</td><td>TMDS_100n</td><td>TMDS</td><td>TMDS DATA N<3..0></td><td>85 94</td></tr><tr><td>TMDS_CLK</td><td>TMDS_100n</td><td>TMDS</td><td>TMDS CLK P</td><td>85 94</td></tr><tr><td>TMDS_100n</td><td>TMDS_100n</td><td>TMDS</td><td>TMDS CLK N</td><td>85 94</td></tr><tr><td>TMDS_100n</td><td>TMDS_100n</td><td>TMDS</td><td>TMDS CONN DP<3..0></td><td>94</td></tr><tr><td>TMDS_100n</td><td>TMDS_100n</td><td>TMDS</td><td>TMDS CONN DN<3..0></td><td>94</td></tr><tr><td>TMDS_100n</td><td>TMDS_100n</td><td>TMDS</td><td>TMDS CONN CLKP</td><td>94</td></tr><tr><td>TMDS_100n</td><td>TMDS_100n</td><td>TMDS</td><td>TMDS CONN CLKN</td><td>94</td></tr><tr><td>(USB_EXT_A)</td><td>USR_90n</td><td>USR</td><td>USB PORT0 P</td><td>46</td></tr><tr><td>(USB_EXT_A)</td><td>USR_90n</td><td>USR</td><td>USB PORT0 N</td><td>46</td></tr><tr><td>(USB_EXTB)</td><td>USR_90n</td><td>USR</td><td>USB PORT1 P</td><td>46</td></tr><tr><td>(USB_EXTB)</td><td>USR_90n</td><td>USR</td><td>USB PORT1 N</td><td>46</td></tr><tr><td>(USB_EXTC)</td><td>USR_90n</td><td>USR</td><td>USB PORT2 P</td><td>46</td></tr><tr><td>(USB_EXTC)</td><td>USR_90n</td><td>USR</td><td>USB PORT2 N</td><td>46</td></tr><tr><td>(USB_EXTD)</td><td>USR_90n</td><td>USR</td><td>USB C MUXED P</td><td>46</td></tr><tr><td>(USB_EXTD)</td><td>USR_90n</td><td>USR</td><td>USB C MUXED N</td><td>46</td></tr><tr><td>(USB_CAMERA)</td><td>USR_90n</td><td>USR</td><td>USB CAMERA L P</td><td>47</td></tr><tr><td>(USB_CAMERA)</td><td>USR_90n</td><td>USR</td><td>USB CAMERA L N</td><td>47</td></tr><tr><td>(USB_IR)</td><td>USR_90n</td><td>USR</td><td>USB IR L P</td><td>47 58</td></tr><tr><td>(USB_IR)</td><td>USR_90n</td><td>USR</td><td>USB IR L N</td><td>47 58</td></tr><tr><td>LVDS_A_CLK</td><td>LVDS_100n</td><td>LVDS</td><td>LVDS L CLK P</td><td>85 90</td></tr><tr><td>LVDS_A_CLK</td><td>LVDS_100n</td><td>LVDS</td><td>LVDS L CLK N</td><td>85 90</td></tr><tr><td>LVDS_A_DATA</td><td>LVDS_100n</td><td>LVDS</td><td>LVDS L DATA P<3..0></td><td>85 90</td></tr><tr><td>LVDS_A_DATA</td><td>LVDS_100n</td><td>LVDS</td><td>LVDS L DATA N<3..0></td><td>85 90</td></tr><tr><td>LVDS_B_CLK</td><td>LVDS_100n</td><td>LVDS</td><td>LVDS U CLK P</td><td>85 90</td></tr><tr><td>LVDS_B_CLK</td><td>LVDS_100n</td><td>LVDS</td><td>LVDS U CLK N</td><td>85 90</td></tr><tr><td>LVDS_B_DATA</td><td>LVDS_100n</td><td>LVDS</td><td>LVDS U DATA P<3..0></td><td>85 90</td></tr><tr><td>LVDS_B_DATA</td><td>LVDS_100n</td><td>LVDS</td><td>LVDS U DATA N<3..0></td><td>85 90</td></tr><tr><td>PCIE_100n</td><td>PCIE</td><td>PCIE</td><td>PCIE FW R2D N</td><td>7 40</td></tr><tr><td>PCIE_100n</td><td>PCIE</td><td>PCIE</td><td>PCIE FW R2D P</td><td>7 40</td></tr><tr><td>PCIE_100n</td><td>PCIE</td><td>PCIE</td><td>PCIE FW D2R C N</td><td>40</td></tr><tr><td>PCIE_100n</td><td>PCIE</td><td>PCIE</td><td>PCIE FW D2R C P</td><td>40</td></tr><tr><td>PCIE_100n</td><td>PCIE</td><td>PCIE</td><td>PCIE ENET R2D P</td><td>7 37</td></tr><tr><td>PCIE_100n</td><td>PCIE</td><td>PCIE</td><td>PCIE ENET R2D N</td><td>7 37</td></tr><tr><td>PCIE_100n</td><td>PCIE</td><td>PCIE</td><td>PCIE ENET D2R C P</td><td>37</td></tr><tr><td>PCIE_100n</td><td>PCIE</td><td>PCIE</td><td>PCIE ENET D2R C N</td><td>37</td></tr><tr><td>PCIE_100n</td><td>PCIE</td><td>PCIE</td><td>PCIE MINI R2D N</td><td>14</td></tr><tr><td>PCIE_100n</td><td>PCIE</td><td>PCIE</td><td>PCIE MINI R2D P</td><td>14</td></tr><tr><td>ENET_MDI_T</td><td>ENET_100n</td><td>ENET_MDI</td><td>ENET MDI T P<0></td><td>39</td></tr><tr><td>ENET_100n</td><td>ENET_MDI</td><td>ENET MDI T N<0></td><td>39</td></tr><tr><td>ENET_MDI_T</td><td>ENET_100n</td><td>ENET_MDI</td><td>ENET MDI T P<1></td><td>39</td></tr><tr><td>ENET_100n</td><td>ENET_MDI</td><td>ENET MDI T N<1></td><td>39</td></tr><tr><td>ENET_MDI_T</td><td>ENET_100n</td><td>ENET_MDI</td><td>ENET MDI T P<2></td><td>39</td></tr><tr><td>ENET_100n</td><td>ENET_MDI</td><td>ENET MDI T N<2></td><td>39</td></tr><tr><td>ENET_MDI_T</td><td>ENET_100n</td><td>ENET_MDI</td><td>ENET MDI T P<3></td><td>39</td></tr><tr><td>ENET_100n</td><td>ENET_MDI</td><td>ENET MDI T N<3></td><td>39</td></tr><tr><td>ENET_100n</td><td>ENET_MDI</td><td>ENET MDI R P<0></td><td></td></tr><tr><td>ENET_100n</td><td>ENET_MDI</td><td>ENET MDI R N<0></td><td></td></tr><tr><td>ENET_100n</td><td>ENET_MDI</td><td>ENET MDI R P<1></td><td></td></tr><tr><td>ENET_100n</td><td>ENET_MDI</td><td>ENET MDI R N<1></td><td></td></tr><tr><td>ENET_100n</td><td>ENET_MDI</td><td>ENET MDI R P<2></td><td></td></tr><tr><td>ENET_100n</td><td>ENET_MDI</td><td>ENET MDI R N<2></td><td></td></tr><tr><td>ENET_100n</td><td>ENET_MDI</td><td>ENET MDI R P<3></td><td></td></tr><tr><td>ENET_100n</td><td>ENET_MDI</td><td>ENET MDI R N<3></td><td></td></tr><tr><td>CRT_50S</td><td>CRT</td><td>CRT</td><td>GPU_TV_COMP</td><td>85 91</td></tr><tr><td>CRT_50S</td><td>CRT</td><td>CRT</td><td>GPU_TV_C</td><td>85 91</td></tr><tr><td>CRT_50S</td><td>CRT</td><td>CRT</td><td>GPU_TV_Y</td><td>85 91</td></tr><tr><td>CRT_50S</td><td>CRT</td><td>CRT</td><td>GPU_RED</td><td>85 91</td></tr><tr><td>CRT_50S</td><td>CRT</td><td>CRT</td><td>GPU_GRN</td><td>85 91</td></tr><tr><td>CRT_50S</td><td>CRT</td><td>CRT</td><td>GPU_BLU</td><td>85 91</td></tr><tr><td>(CRT_SYNC)</td><td>CRT_55S</td><td>CRT_SYNC</td><td>GPU_H2SYNC</td><td>85 91</td></tr><tr><td>(CRT_SYNC)</td><td>CRT_55S</td><td>CRT_SYNC</td><td>GPU_V2SYNC</td><td>85 91</td></tr><tr><td>CRT_SYNC</td><td>CRT_55S</td><td>CRT_SYNC</td><td>VGA_HSYNC</td><td>91 94</td></tr><tr><td>CRT_SYNC</td><td>CRT_55S</td><td>CRT_SYNC</td><td>VGA_VSYNC</td><td>91 94</td></tr><tr><td>(CRT_SYNC)</td><td>CRT_55S</td><td>CRT_SYNC</td><td>GPU_BUF_HSYNC</td><td></td></tr><tr><td>(CRT_SYNC)</td><td>CRT_55S</td><td>CRT_SYNC</td><td>GPU_BUF_VSYNC</td><td></td></tr><tr><td>CRT_50S</td><td>CRT</td><td>CRT</td><td>VIDEO_MUX_RED</td><td>91</td></tr><tr><td>CRT_50S</td><td>CRT</td><td>CRT</td><td>VIDEO_MUX_GRN</td><td>91</td></tr><tr><td>CRT_50S</td><td>CRT</td><td>CRT</td><td>VIDEO_MUX_BLU</td><td>91</td></tr><tr><td>CRT_55S</td><td>CRT</td><td>CRT</td><td>VGA_RED</td><td>91 94</td></tr><tr><td>CRT_55S</td><td>CRT</td><td>CRT</td><td>VGA_GRN</td><td>91 94</td></tr><tr><td>CRT_55S</td><td>CRT</td><td>CRT</td><td>VGA_BLU</td><td>91 94</td></tr><tr><td>THERM_DIFF</td><td>THERM_DIFF</td><td>THERMAL</td><td>HDD_THRMD_P</td><td>55</td></tr><tr><td>THERM_DIFF</td><td>THERM_DIFF</td><td>THERMAL</td><td>HDD_THRMD_N</td><td>55</td></tr><tr><td>THERM_DIFF</td><td>THERM_DIFF</td><td>THERMAL</td><td>ODD_THRMD_P</td><td>55</td></tr><tr><td>THERM_DIFF</td><td>THERM_DIFF</td><td>THERMAL</td><td>ODD_THRMD_N</td><td>55</td></tr><tr><td>THERM_DIFF</td><td>THERM_DIFF</td><td>THERMAL</td><td>CPU_THRMD_P</td><td>10 55</td></tr><tr><td>THERM_DIFF</td><td>THERM_DIFF</td><td>THERMAL</td><td>CPU_THRMD_N</td><td>10 55</td></tr><tr><td>THERM_DIFF</td><td>THERM_DIFF</td><td>THERMAL</td><td>GPU_HSK_THRMD_P</td><td>55</td></tr><tr><td>THERM_DIFF</td><td>THERM_DIFF</td><td>THERMAL</td><td>GPU_HSK_THRMD_N</td><td>55</td></tr><tr><td>THERM_DIFF</td><td>THERM_DIFF</td><td>THERMAL</td><td>CPU_HSK_THRMD_P</td><td>55</td></tr><tr><td>THERM_DIFF</td><td>THERM_DIFF</td><td>THERMAL</td><td>CPU_HSK_THRMD_N</td><td>55</td></tr></table>								ELECTRICAL_CONSTRAINT_SET	NET_TYPE				PHYSICAL	SPACING	TMDS_DATA	TMDS_100n	TMDS	TMDS DATA P<3..0>	85 94	TMDS_100n	TMDS_100n	TMDS	TMDS DATA N<3..0>	85 94	TMDS_CLK	TMDS_100n	TMDS	TMDS CLK P	85 94	TMDS_100n	TMDS_100n	TMDS	TMDS CLK N	85 94	TMDS_100n	TMDS_100n	TMDS	TMDS CONN DP<3..0>	94	TMDS_100n	TMDS_100n	TMDS	TMDS CONN DN<3..0>	94	TMDS_100n	TMDS_100n	TMDS	TMDS CONN CLKP	94	TMDS_100n	TMDS_100n	TMDS	TMDS CONN CLKN	94	(USB_EXT_A)	USR_90n	USR	USB PORT0 P	46	(USB_EXT_A)	USR_90n	USR	USB PORT0 N	46	(USB_EXTB)	USR_90n	USR	USB PORT1 P	46	(USB_EXTB)	USR_90n	USR	USB PORT1 N	46	(USB_EXTC)	USR_90n	USR	USB PORT2 P	46	(USB_EXTC)	USR_90n	USR	USB PORT2 N	46	(USB_EXTD)	USR_90n	USR	USB C MUXED P	46	(USB_EXTD)	USR_90n	USR	USB C MUXED N	46	(USB_CAMERA)	USR_90n	USR	USB CAMERA L P	47	(USB_CAMERA)	USR_90n	USR	USB CAMERA L N	47	(USB_IR)	USR_90n	USR	USB IR L P	47 58	(USB_IR)	USR_90n	USR	USB IR L N	47 58	LVDS_A_CLK	LVDS_100n	LVDS	LVDS L CLK P	85 90	LVDS_A_CLK	LVDS_100n	LVDS	LVDS L CLK N	85 90	LVDS_A_DATA	LVDS_100n	LVDS	LVDS L DATA P<3..0>	85 90	LVDS_A_DATA	LVDS_100n	LVDS	LVDS L DATA N<3..0>	85 90	LVDS_B_CLK	LVDS_100n	LVDS	LVDS U CLK P	85 90	LVDS_B_CLK	LVDS_100n	LVDS	LVDS U CLK N	85 90	LVDS_B_DATA	LVDS_100n	LVDS	LVDS U DATA P<3..0>	85 90	LVDS_B_DATA	LVDS_100n	LVDS	LVDS U DATA N<3..0>	85 90	PCIE_100n	PCIE	PCIE	PCIE FW R2D N	7 40	PCIE_100n	PCIE	PCIE	PCIE FW R2D P	7 40	PCIE_100n	PCIE	PCIE	PCIE FW D2R C N	40	PCIE_100n	PCIE	PCIE	PCIE FW D2R C P	40	PCIE_100n	PCIE	PCIE	PCIE ENET R2D P	7 37	PCIE_100n	PCIE	PCIE	PCIE ENET R2D N	7 37	PCIE_100n	PCIE	PCIE	PCIE ENET D2R C P	37	PCIE_100n	PCIE	PCIE	PCIE ENET D2R C N	37	PCIE_100n	PCIE	PCIE	PCIE MINI R2D N	14	PCIE_100n	PCIE	PCIE	PCIE MINI R2D P	14	ENET_MDI_T	ENET_100n	ENET_MDI	ENET MDI T P<0>	39	ENET_100n	ENET_MDI	ENET MDI T N<0>	39	ENET_MDI_T	ENET_100n	ENET_MDI	ENET MDI T P<1>	39	ENET_100n	ENET_MDI	ENET MDI T N<1>	39	ENET_MDI_T	ENET_100n	ENET_MDI	ENET MDI T P<2>	39	ENET_100n	ENET_MDI	ENET MDI T N<2>	39	ENET_MDI_T	ENET_100n	ENET_MDI	ENET MDI T P<3>	39	ENET_100n	ENET_MDI	ENET MDI T N<3>	39	ENET_100n	ENET_MDI	ENET MDI R P<0>		ENET_100n	ENET_MDI	ENET MDI R N<0>		ENET_100n	ENET_MDI	ENET MDI R P<1>		ENET_100n	ENET_MDI	ENET MDI R N<1>		ENET_100n	ENET_MDI	ENET MDI R P<2>		ENET_100n	ENET_MDI	ENET MDI R N<2>		ENET_100n	ENET_MDI	ENET MDI R P<3>		ENET_100n	ENET_MDI	ENET MDI R N<3>		CRT_50S	CRT	CRT	GPU_TV_COMP	85 91	CRT_50S	CRT	CRT	GPU_TV_C	85 91	CRT_50S	CRT	CRT	GPU_TV_Y	85 91	CRT_50S	CRT	CRT	GPU_RED	85 91	CRT_50S	CRT	CRT	GPU_GRN	85 91	CRT_50S	CRT	CRT	GPU_BLU	85 91	(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_H2SYNC	85 91	(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_V2SYNC	85 91	CRT_SYNC	CRT_55S	CRT_SYNC	VGA_HSYNC	91 94	CRT_SYNC	CRT_55S	CRT_SYNC	VGA_VSYNC	91 94	(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_BUF_HSYNC		(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_BUF_VSYNC		CRT_50S	CRT	CRT	VIDEO_MUX_RED	91	CRT_50S	CRT	CRT	VIDEO_MUX_GRN	91	CRT_50S	CRT	CRT	VIDEO_MUX_BLU	91	CRT_55S	CRT	CRT	VGA_RED	91 94	CRT_55S	CRT	CRT	VGA_GRN	91 94	CRT_55S	CRT	CRT	VGA_BLU	91 94	THERM_DIFF	THERM_DIFF	THERMAL	HDD_THRMD_P	55	THERM_DIFF	THERM_DIFF	THERMAL	HDD_THRMD_N	55	THERM_DIFF	THERM_DIFF	THERMAL	ODD_THRMD_P	55	THERM_DIFF	THERM_DIFF	THERMAL	ODD_THRMD_N	55	THERM_DIFF	THERM_DIFF	THERMAL	CPU_THRMD_P	10 55	THERM_DIFF	THERM_DIFF	THERMAL	CPU_THRMD_N	10 55	THERM_DIFF	THERM_DIFF	THERMAL	GPU_HSK_THRMD_P	55	THERM_DIFF	THERM_DIFF	THERMAL	GPU_HSK_THRMD_N	55	THERM_DIFF	THERM_DIFF	THERMAL	CPU_HSK_THRMD_P	55	THERM_DIFF	THERM_DIFF	THERMAL	CPU_HSK_THRMD_N	55
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M72/M78 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS																	
BOARD LAYERS				BOARD AREAS				BOARD UNITS (MIL or MM)		ALLEGRO VERSION							
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, BOTTOM				NO_TYPE, BGA_P1MM				MM		15.5.1							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	4 MM	0 MM	0 MM										
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT										
DEFAULT	TOP, BOTTOM	Y	=55_OHM_SE	0.100 MM	3 MM	0 MM	0 MM										
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
55_OHM_SE	TOP, BOTTOM	Y	0.125 MM	0.125 MM													
55_OHM_SE	*	Y	0.100 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD										
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
40_OHM_SE	TOP, BOTTOM	Y	0.225 MM	0.225 MM													
40_OHM_SE	*	Y	0.185 MM	0.185 MM	=STANDARD	=STANDARD	=STANDARD										
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
45_OHM_SE	TOP, BOTTOM	Y	0.185 MM	0.185 MM													
45_OHM_SE	*	Y	0.150 MM	0.150 MM	=STANDARD	=STANDARD	=STANDARD										
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
27P4_OHM_SE	TOP, BOTTOM	Y	0.340 MM	0.340 MM													
27P4_OHM_SE	*	Y	0.265 MM	0.265 MM	=STANDARD	=STANDARD	=STANDARD										
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD										
70_OHM_DIFF	ISL3, ISL6	Y	0.180 MM	0.180 MM		0.120 MM	0.120 MM										
70_OHM_DIFF	TOP, BOTTOM	Y	0.215 MM	0.215 MM		0.125 MM	0.125 MM										
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD										
85_OHM_DIFF	ISL3, ISL6	Y	0.120 MM	0.120 MM		0.130 MM	0.130 MM										
85_OHM_DIFF	TOP, BOTTOM	Y	0.145 MM	0.145 MM		0.125 MM	0.125 MM										
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD										
90_OHM_DIFF	ISL3, ISL6	Y	0.125 MM	0.125 MM		0.200 MM	0.200 MM										
90_OHM_DIFF	TOP, BOTTOM	Y	0.145 MM	0.145 MM		0.175 MM	0.175 MM										
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD										
100_OHM_DIFF	ISL3, ISL6	Y	0.095 MM	0.095 MM		0.205 MM	0.205 MM										
100_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM										
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD										
110_OHM_DIFF	ISL3, ISL6	Y	0.085 MM	0.085 MM		0.330 MM	0.330 MM										
110_OHM_DIFF	TOP, BOTTOM	Y	0.105 MM	0.100 MM		0.280 MM	0.280 MM										
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM										
SPACING_RULE_SET				LAYER		LINE-TO-LINE SPACING		WEIGHT		NET_SPACING_TYPE1		NET_SPACING_TYPE2		AREA_TYPE		SPACING_RULE_SET	
DEFAULT				*		0.1 MM		?		*		*		BGA_P1MM		BGA_P1MM	
STANDARD				*		=DEFAULT		?		MEM_CLK		*		BGA_P1MM		BGA_P2MM	
BGA_P1MM				*		=DEFAULT		?		CLK_FSB		*		BGA_P1MM		BGA_P2MM	
BGA_P2MM				*		=DEFAULT		?		CLK_PCIE		*		BGA_P1MM		BGA_P2MM	
BGA_P3MM				*		=DEFAULT		?		CLK_MED		*		BGA_P1MM		BGA_P2MM	
SPACING_RULE_SET				LAYER		LINE-TO-LINE SPACING		WEIGHT		FSB_DSTB		FSB_DSTB		BGA_P1MM		BGA_P3MM	
SPACING_0.15MM				*		0.15 MM		?									
SPACING_0.18MM				*		0.18 MM		?									
SPACING_0.2MM				*		0.2 MM		?									
SPACING_0.25MM				*		0.25 MM		?		CLK_SPACING_0.5MM		*		0.5 MM		?	
SPACING_0.3MM				*		0.3 MM		?		CLK_SPACING_0.6MM		*		0.6 MM		?	
SPACING_0.4MM				*		0.4 MM		?		CLK_SPACING_0.5MM		TOP, BOTTOM		0.2 MM		?	
SPACING_0.5MM				*		0.5 MM		?		CLK_SPACING_0.6MM		TOP, BOTTOM		0.2 MM		?	
SPACING_0.6MM				*		0.6 MM		?									
SWITCHNODE				*		0.6 MM		1000									
SWITCHNODE				TOP, BOTTOM		0.2 MM		1000									

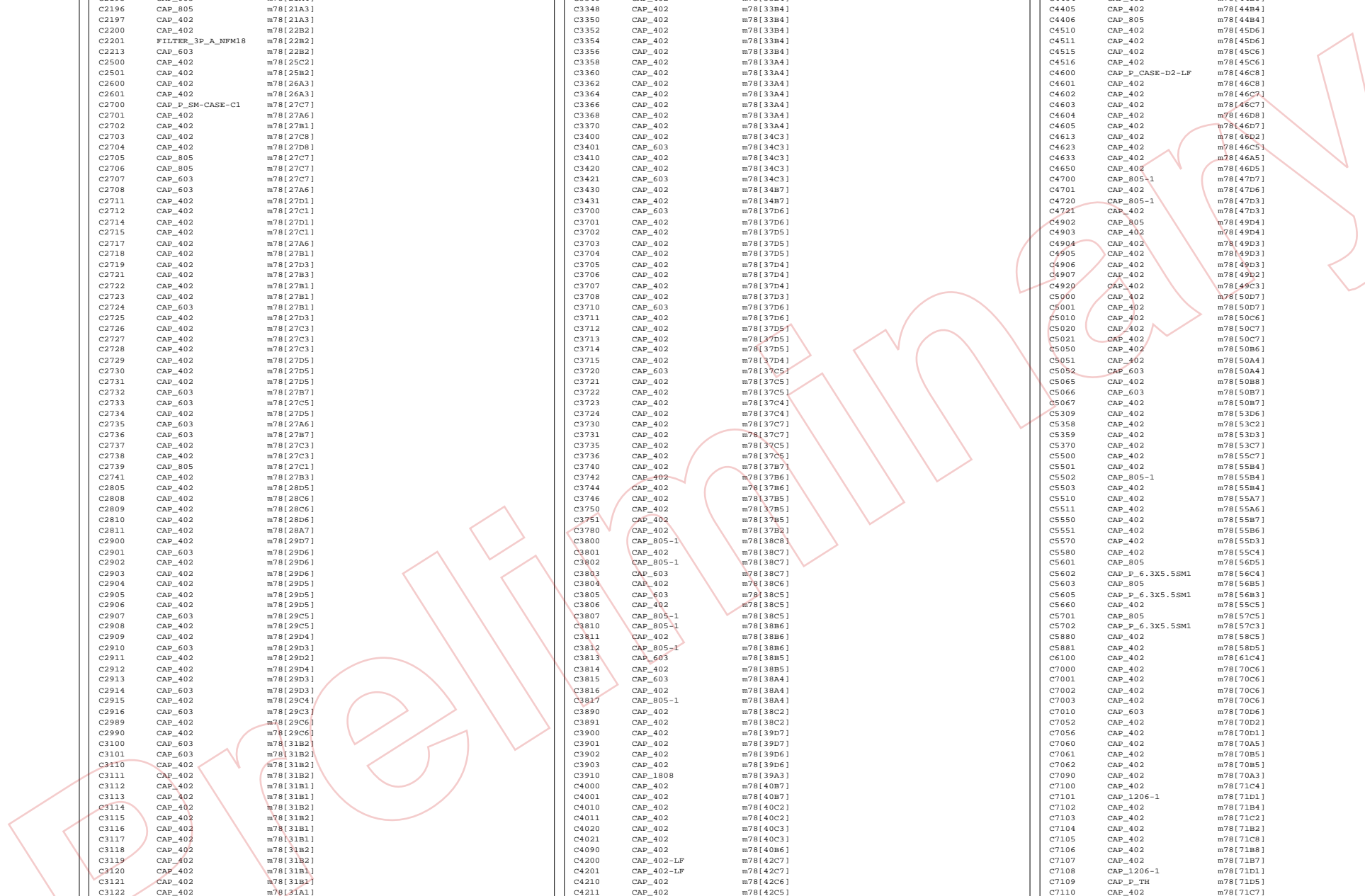
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	8	7	6	5	4	3	2	1	
D	CK505_LVDS_P	CK505_LVDS_P - @m78_lib.M78	29B3 30C5 105D3	DMI_S2N_P<0>	DMI_S2N_P<0> - @m78_lib.M78	7C7 16B3 24D2 101C3	FW_PORT0_TPB_N	FW_PORT0_TPB_N - @m78_lib.M78	43C5 43C6 106D3
	CK505_PCI1_CLK	TP_CK505_LVDS_P - @m78_lib.M78	30C3	DMI_S2N_P<1>	DMI_S2N_P<1> - @m78_lib.M78	16B3 24D2	FW_P0_TPB_N	FW_P0_TPB_N - @m78_lib.M78	40C6 43C8
	CK505_PCI1_CLK	CK505_PCI1_CLK - @m78_lib.M78	29C5 30A5 105D3	DMI_S2N_P<3..1>	DMI_S2N_P<3..1> - @m78_lib.M78	101D3	FW_PORT0_TPB_P	FW_PORT0_TPB_P - @m78_lib.M78	43C5 43C6 106D3
	CK505_PCI2_CLK	TP_CK505_PCI1_CLK - @m78_lib.M78	7C3 30A3	DMI_S2N_P<2>	DMI_S2N_P<2> - @m78_lib.M78	16B3 24D2	FW_P0_TPB_P	FW_P0_TPB_P - @m78_lib.M78	40C6 43C8
	CK505_PCI2_CLK	CK505_PCI2_CLK - @m78_lib.M78	29B5 30A5 105D3	DMI_S2N_P<3>	DMI_S2N_P<3> - @m78_lib.M78	16B3 24D2	FW_PORT0_VP	FW_PORT0_VP - @m78_lib.M78	43D3
	CK505_PCI3_CLK	TP_PCI_CLK33M_TPM - @m78_lib.M78	30A3	DVI_DDC_CLK	DVI_DDC_CLK - @m78_lib.M78	94D2	FW_PORT0_VP_F	FW_PORT0_VP_F - @m78_lib.M78	43D5
	CK505_PCI3_CLK	CK505_PCI3_CLK - @m78_lib.M78	29B5 30A5 105D3	DVI_DDC_CLK_UP	DVI_DDC_CLK_UP - @m78_lib.M78	94D3 94D5	FW_PORT1_TPA_FL_N	FW_PORT1_TPA_FL_N - @m78_lib.M78	43B2 106D3
	CK505_PCI4_CLK	CK505_PCI4_CLK - @m78_lib.M78	29B5 30A5 105D3	DVI_DDC_DATA	DVI_DDC_DATA - @m78_lib.M78	94C2	FW_PORT1_TPA_FL_P	FW_PORT1_TPA_FL_P - @m78_lib.M78	43B2 106D3
	CK505_PCI4_CLK	TP_CK505_PCI4_CLK - @m78_lib.M78	30A3	DVI_DDC_DATA_UP	DVI_DDC_DATA_UP - @m78_lib.M78	94C3 94D5	FW_PORT1_TPA_N	FW_PORT1_TPA_N - @m78_lib.M78	43B6 43C6 106D3
	CK505_PCI5_CLK_FCTSE	CK505_PCI5_CLK_FCTSEL - @m78_lib.M78	29B5 30D8 105D3	DVI_HOTPLUG_DET	DVI_HOTPLUG_DET - @m78_lib.M78	24A6 24B2	FW_PL_TPA_N	FW_PL_TPA_N - @m78_lib.M78	40C6 43C8
C	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	SV_GPI04 - @m78_lib.M78	SV_GPI04 - @m78_lib.M78	28B2	FW_PORT1_TPA_P	FW_PORT1_TPA_P - @m78_lib.M78	43B6 43C6 106D3
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	DVI_HPD_UP	DVI_HPD_UP - @m78_lib.M78	94C3 94D5	FW_PL_TPA_P	FW_PL_TPA_P - @m78_lib.M78	40C6 43C8
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_CLK25M_XTALI	ENET_CLK25M_XTALI - @m78_lib.M78	37B4	FW_PORT1_TPB_FL_N	FW_PORT1_TPB_FL_N - @m78_lib.M78	43B2 106D3
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_CLK25M_XTALO	ENET_CLK25M_XTALO - @m78_lib.M78	37B4	FW_PORT1_TPB_FL_P	FW_PORT1_TPB_FL_P - @m78_lib.M78	43B2 106D3
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_CTAP<0>	ENET_CTAP<0> - @m78_lib.M78	39B5	FW_PORT1_TPB_N	FW_PORT1_TPB_N - @m78_lib.M78	43A6 43C6 106D3
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_CTAP<1>	ENET_CTAP<1> - @m78_lib.M78	39B5	FW_PL_TPB_N	FW_PL_TPB_N - @m78_lib.M78	40C6 43C8
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_CTAP<2>	ENET_CTAP<2> - @m78_lib.M78	39B5	FW_PL_TPB_P	FW_PL_TPB_P - @m78_lib.M78	43B6 43C6 106D3
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_CTAP<3>	ENET_CTAP<3> - @m78_lib.M78	39A5	FW_PORT1_VP	FW_PORT1_VP - @m78_lib.M78	43B3
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_CTAP_COMMON	ENET_CTAP_COMMON - @m78_lib.M78	39A4	FW_PORT1_VP_F	FW_PORT1_VP_F - @m78_lib.M78	43D5
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_CTRL12	ENET_CTRL12 - @m78_lib.M78	38A5 38B1	FW_PORTS_VP	FW_PORTS_VP - @m78_lib.M78	43D7
B	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	TP_YUKON_CTRL12	TP_YUKON_CTRL12 - @m78_lib.M78	37C2 38B3	FW_PORTS_VP_R	FW_PORTS_VP_R - @m78_lib.M78	40C7 43D6
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_CTRL19R25	ENET_CTRL19R25 - @m78_lib.M78	38B1 38C6	FW_PU_RST_L	FW_PU_RST_L - @m78_lib.M78	40B6
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	TP_YUKON_CTRL18	TP_YUKON_CTRL18 - @m78_lib.M78	37C2 38B3	FW_R0	FW_R0 - @m78_lib.M78	40B6
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_LED_ACT_L	ENET_LED_ACT_L - @m78_lib.M78	37B2 39A8	FW_RESET_L	FW_RESET_L - @m78_lib.M78	7D6 28C1 40B3
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_LED_LINK10_100_L	ENET_LED_LINK10_100_L - @m78_lib.M78	37B2 39A8	FW_REXT	FW_REXT - @m78_lib.M78	40B6
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_LED_LINK1000_L	ENET_LED_LINK1000_L - @m78_lib.M78	37B2 39A8	FW_SCD	FW_SCD - @m78_lib.M78	40B6
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_LED_LINK_L	ENET_LED_LINK_L - @m78_lib.M78	37C2	FW_TPCDS	FW_TPCDS - @m78_lib.M78	40B6
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_LOM_DIS_L	ENET_LOM_DIS_L - @m78_lib.M78	37C2	FW_TRST_L	FW_TRST_L - @m78_lib.M78	7C3 40C3
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_MD10	ENET_MD10 - @m78_lib.M78	37B7 104B3	FW_VAUX_DETECT	FW_VAUX_DETECT - @m78_lib.M78	40C3
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_MD11	ENET_MD11 - @m78_lib.M78	37B6 104B3	FW_XI	FW_XI - @m78_lib.M78	40B6
A	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_MD12	ENET_MD12 - @m78_lib.M78	37B6 104B3	FW_XO	FW_XO - @m78_lib.M78	40B6
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_MD13	ENET_MD13 - @m78_lib.M78	37B5 104B3	FW_XO_R	FW_XO_R - @m78_lib.M78	40B7
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_MD1_N<0>	ENET_MD1_N<0> - @m78_lib.M78	37B8 39C7 104B3	GATE_12V_S3	GATE_12V_S3 - @m78_lib.M78	7B2D
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_MD1_N<1>	ENET_MD1_N<1> - @m78_lib.M78	37B8 39C7 104B3	GATE_12V_S3_R	GATE_12V_S3_R - @m78_lib.M78	7B2D
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_MD1_N<2>	ENET_MD1_N<2> - @m78_lib.M78	37B8 39B7 104A3	GPX_VID<1>	GPX_VID<1> - @m78_lib.M78	16B3 22B8
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_MD1_N<3>	ENET_MD1_N<3> - @m78_lib.M78	37B8 39B7 104A3	GPX_VID<2>	GPX_VID<2> - @m78_lib.M78	16B3 22A8
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_MD1_P<0>	ENET_MD1_P<0> - @m78_lib.M78	37B8 39C7 104B3	GPX_VID<3>	GPX_VID<3> - @m78_lib.M78	16B3 22A8
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_MD1_P<1>	ENET_MD1_P<1> - @m78_lib.M78	37B8 39C7 104B3	GPX_VID<4>	GPX_VID<4> - @m78_lib.M78	16B3 22A8
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_MD1_P<2>	ENET_MD1_P<2> - @m78_lib.M78	37B8 39B7 104B3	GLAN_COMP	GLAN_COMP - @m78_lib.M78	23C6 104B3
	CK505_PCI5_CLK_ITFE	CK505_PCI5_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3	ENET_MD1_P<3>	ENET_MD1_P<3> - @m78_lib.M78	37B8 39B7 104A3	GND_IMVP6_SGND	GND_IMVP6_SGND - @m78_lib.M78	71B6

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D	Title: Cref Part Report Design: m78 Date: May 7 18:11:37 2007																							
	C600	CAP_402	m78[6D7]	C2171	CAP_402-1	m78[21D4]	C3305	CAP_402	m78[33D4]	C4312	CAP_402	m78[43C4]												
	C621	CAP_603	m78[6D6]	C2173	CAP_P_SM-CASE-C1	m78[21C4]	C3307	CAP_402	m78[33D4]	C4313	CAP_402	m78[43C4]												
	C622	CAP_805	m78[6D7]	C2174	CAP_603	m78[21C4]	C3310	CAP_402	m78[33C4]	C4320	CAP_402	m78[43B5]												
	C623	CAP_805	m78[6D7]	C2177	CAP_603	m78[21C4]	C3312	CAP_402	m78[33C4]	C4321	CAP_402	m78[43B5]												
	C624	CAP_1210	m78[6D8]	C2180	CAP_402	m78[21D2]	C3330	CAP_402	m78[33C4]	C4322	CAP_402	m78[43A5]												
	C625	CAP_P_6_3X5.5-SM	m78[6D8]	C2181	CAP_805	m78[21D2]	C3332	CAP_402	m78[33C4]	C4323	CAP_402	m78[43A5]												
	C701	CAP_402	m78[7C6]	C2182	CAP_402	m78[21D2]	C3334	CAP_402	m78[33C4]	C4332	CAP_402	m78[43C2]												
	C702	CAP_402	m78[7C5]	C2183	CAP_805	m78[21C3]	C3336	CAP_402	m78[33C4]	C4335	CAP_603-1	m78[43C2]												
	C703	CAP_402	m78[7C6]	C2184	CAP_402	m78[21C2]	C3338	CAP_402	m78[33C4]	C4350	CAP_402	m78[43C7]												
C	C704	CAP_402	m78[7C5]	C2190	CAP_603	m78[21B4]	C3340	CAP_402	m78[33C4]	C4354	CAP_402	m78[43B7]												
	C705	CAP_402	m78[7C6]	C2191	CAP_402	m78[21B3]	C3342	CAP_402	m78[33B4]	C4360	CAP_402	m78[43D7]												
	C706	CAP_402	m78[7B5]	C2192	CAP_402	m78[21B3]	C3344	CAP_402	m78[33B4]	C4364	CAP_402	m78[43B7]												
	C707	CAP_402	m78[7B6]	C2195	CAP_603	m78[21A4]	C3346	CAP_402	m78[33B4]	C4404	CAP_402	m78[44B6]												
	C708	CAP_402	m78[7B5]	C2196	CAP_805	m78[21A3]	C3348	CAP_402	m78[33B4]	C4405	CAP_402	m78[44B4]												
	C709	CAP_402	m78[7B6]	C2197	CAP_402	m78[21A3]	C3350	CAP_402	m78[33B4]	C4406	CAP_805	m78[44B4]												
	C710	CAP_402	m78[7B5]	C2200	CAP_402	m78[22B2]	C3352	CAP_402	m78[33B4]	C4510	CAP_402	m78[45D6]												
	C1000	CAP_402	m78[10B5]	C2201	FILTER_3P_A_NFM18	m78[22B2]	C3354	CAP_402	m78[33B4]	C4511	CAP_402	m78[45D6]												
	C1200	CAP_805	m78[12D7]	C2213	CAP_603	m78[22B2]	C3356	CAP_402	m78[33B4]	C4515	CAP_402	m78[45C6]												
	C1201	CAP_805	m78[12D6]	C2500	CAP_402	m78[25C2]	C3358	CAP_402	m78[33A4]	C4516	CAP_402	m78[45C6]												
B	C1202	CAP_805	m78[12D6]	C2501	CAP_402	m78[25B2]	C3360	CAP_402	m78[33A4]	C4600	CAP_P_CASE-D2-LF	m78[46C8]												
	C1203	CAP_805	m78[12D6]	C2600	CAP_402	m78[26A3]	C3362	CAP_402	m78[33A4]	C4601	CAP_402	m78[46C8]												
	C1204	CAP_805	m78[12D6]	C2601	CAP_402	m78[26A3]	C3364	CAP_402	m78[33A4]	C4602	CAP_402	m78[46C7]												
	C1205	CAP_805	m78[12D5]	C2700	CAP_P_SM-CASE-C1	m78[27C7]	C3366	CAP_402	m78[33A4]	C4603	CAP_402	m78[46C7]												
	C1206	CAP_805	m78[12D5]	C2701	CAP_402	m78[27A6]	C3368	CAP_402	m78[33A4]	C4604	CAP_402	m78[46D8]												
	C1207	CAP_805	m78[12D5]	C2702	CAP_402	m78[27B1]	C3370	CAP_402	m78[33A4]	C4605	CAP_402	m78[46D7]												
	C1208	CAP_805	m78[12D4]	C2703	CAP_402	m78[27C8]	C3400	CAP_402	m78[34C3]	C4613	CAP_402	m78[46D2]												
	C1209	CAP_805	m78[12D4]	C2704	CAP_402	m78[27D8]	C3401	CAP_603	m78[34C3]	C4623	CAP_402	m78[46C5]												
	C1210	CAP_805	m78[12C7]	C2705	CAP_805	m78[27C7]	C3410	CAP_402	m78[34C3]	C4633	CAP_402	m78[46A5]												
	C1211	CAP_805	m78[12C6]	C2706	CAP_805	m78[27C7]	C3420	CAP_402	m78[34C3]	C4650	CAP_402	m78[46D5]												
A	C1212	CAP_805	m78[12C6]	C2707	CAP_603	m78[27C7]	C3421	CAP_603	m78[34C3]	C4700	CAP_805-1	m78[47D7]												
	C1213	CAP_805	m78[12C6]	C2708	CAP_603	m78[27A6]	C3430	CAP_402	m78[34B7]	C4701	CAP_402	m78[47D6]												
	C1214	CAP_805	m78[12C6]	C2711	CAP_402	m78[27D1]	C3431	CAP_402	m78[34B7]	C4720	CAP_805-1	m78[47D3]												
	C1215	CAP_805	m78[12C5]	C2712	CAP_402	m78[27C1]	C3700	CAP_603	m78[37D6]	C4721	CAP_402	m78[47D3]												
	C1216	CAP_805	m78[12C5]	C2714	CAP_402	m78[27D1]	C3701	CAP_402	m78[37D6]	C4902	CAP_805	m78[49D4]												
	C1217	CAP_805	m78[12C5]	C2715	CAP_402	m78[27C1]	C3702	CAP_402	m78[37D5]	C4903	CAP_402	m78[49D4]												
	C1218	CAP_805	m78[12C4]	C2717	CAP_402	m78[27A6]	C3703	CAP_402	m78[37D5]	C4904	CAP_402	m78[49D3]												
	C1219	CAP_805	m78[12C4]	C2718	CAP_402	m78[27B1]	C3704	CAP_402	m78[37D5]	C4905	CAP_402	m78[49D3]												
	C1220	CAP_805	m78[12C7]	C2719	CAP_402	m78[27D3]	C3705	CAP_402	m78[37D4]	C4906	CAP_402	m78[49D3]												
	C1221	CAP_805	m78[12C6]	C2721	CAP_402	m78[27B3]	C3706	CAP_402	m78[37D4]	C4907	CAP_402	m78[49D2]												

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D	C7201	CAP_1206-1	m78[72D2]	C7203	CAP_402	m78[72C2]	C7208	CAP_1206-1	m78[72D2]	C7212	CAP_402	m78[72C3]	C7215	CAP_603	m78[72C5]	C7235	CAP_603	m78[72D6]	C7254	CAP_P_TH	m78[72D2]	C7255	CAP_1206-1	m78[72D2]	C7290	CAP_402	m78[72C4]	C7300	CAP_P_CASE-D2-SM	m78[73C8]	C7301	CAP_805	m78[73C8]	C7302	CAP_402	m78[73B7]	C7303	CAP_P_CASE-D2-SM	m78[73C7]	C7304	CAP_805	m78[73C8]	C7310	CAP_603	m78[73C7]	C7324	CAP_402	m78[73B7]	C7330	CAP_603-1	m78[73D6]	C7331	CAP_603	m78[73C6]	C7332	CAP_402	m78[73B5]	C7335	CAP_402	m78[73B6]	C7340	CAP_P_TH	m78[73D7]	C7341	CAP_1206-1	m78[73D7]	C7342	CAP_1206-1	m78[73D6]	C7345	CAP_402	m78[73B3]	C7360	CAP_603	m78[73D2]	C7361	CAP_603	m78[73C2]	C7364	CAP_402	m78[73B2]	C7370	CAP_402	m78[73B2]	C7372	CAP_402	m78[73B4]	C7381	CAP_1206-1	m78[73D2]	C7382	CAP_1206-1	m78[73D2]	C7390	CAP_P_CASE-D2-SM	m78[73C1]	C7391	CAP_P_CASE-D2-SM	m78[73C2]	C7392	CAP_805	m78[73C1]	C7393	CAP_805	m78[73C1]	C7400	CAP_P_CASE-D2-SM	m78[74C8]	C7401	CAP_805	m78[74C8]	C7402	CAP_402	m78[74B7]	C7403	CAP_P_CASE-D2-SM	m78[74C7]	C7404	CAP_805	m78[74C8]	C7410	CAP_603	m78[74C7]	C7424	CAP_402	m78[74B7]	C7430	CAP_603-1	m78[74D6]	C7431	CAP_603	m78[74C6]	C7432	CAP_402	m78[74B5]	C7435	CAP_402	m78[74B6]	C7440	CAP_P_TH	m78[74D7]	C7441	CAP_1206-1	m78[74D7]	C7442	CAP_1206-1	m78[74D6]	C7445	CAP_402	m78[74B3]	C7460	CAP_603-1	m78[74D2]	C7461	CAP_603	m78[74C2]	C7464	CAP_402	m78[74B2]	C7470	CAP_402	m78[74B2]	C7472	CAP_402	m78[74B4]	C7480	CAP_P_TH	m78[74D3]	C7481	CAP_1206-1	m78[74D2]	C7482	CAP_1206-1	m78[74D2]	C7490	CAP_P_TH	m78[74C2]	C7491	CAP_P_TH	m78[74C1]	C7492	CAP_805	m78[74C1]	C7493	CAP_805	m78[74C1]	C7500	CAP_603	m78[75D5]	C7501	CAP_603	m78[75D6]	C7502	CAP_603	m78[75D6]	C7503	CAP_402	m78[75C2]	C7506	CAP_402	m78[75C8]	C7507	CAP_402	m78[75C6]	C7508	CAP_603	m78[75C7]	C7509	CAP_402	m78[75D4]	C7510	CAP_402	m78[75C5]	C7530	CAP_P_TH	m78[75D5]	C7531	CAP_603	m78[75D4]	C7532	CAP_P_TH	m78[75D5]	C7533	CAP_1206-1	m78[75D5]	C7534	CAP_1206-1	m78[75D4]	C7540	CAP_805	m78[75C3]	C7541	CAP_805	m78[75C3]	C7542	CAP_P_CASE-D2-SM	m78[75C2]	C7543	CAP_P_CASE-D2-SM	m78[75C2]	C7544	CAP_P_CASE-D2-SM	m78[75C2]	C7550	CAP_402	m78[75B4]	C7551	CAP_805-1	m78[75A6]	C7552	CAP_805-1	m78[75A4]	C7553	CAP_402	m78[75A6]	C7555	CAP_P_CASE-C3	m78[75A4]	C7559	CAP_603	m78[75B5]	C7560	CAP_402	m78[75D8]	C7564	CAP_402	m78[75C3]	C7585	CAP_402	m78[75A3]	C7586	CAP_402	m78[75A2]	C7587	CAP_402	m78[75A2]	C7588	CAP_402	m78[75A2]	C7589	CAP_402	m78[75A1]	C7590	CAP_402	m78[75B3]	C7591	CAP_402	m78[75B2]	C7592	CAP_402	m78[75B2]	C7593	CAP_402	m78[75B2]	C7594	CAP_402	m78[75B1]	C7595	CAP_402	m78[75B3]	C7596	CAP_402	m78[75B2]	C7597	CAP_402	m78[75B2]	C7598	CAP_402	m78[75B2]	C7599	CAP_402	m78[75B1]	C7600	CAP_603	m78[76C4]	C7601	CAP_603	m78[76A4]	C7602	CAP_402	m78[76A4]	C7604	CAP_402	m78[76A3]	C7605	CAP_402	m78[76B5]	C7607	CAP_402	m78[76A3]	C7608	CAP_402	m78[76D2]	C7609	CAP_402	m78[76D7]	C7612	CAP_603	m78[76A7]	C7613	CAP_402	m78[76A7]	C7621	CAP_402	m78[76B6]	C7622	CAP_402	m78[76C5]	C7624	CAP_402	m78[76C6]	C7625	CAP_402	m78[76B6]	C7626	CAP_402	m78[76B6]	C7628	CAP_402	m78[76B7]	C7629	CAP_402	m78[76B7]	C7630	CAP_402	m78[76A5]	C7631	CAP_402	m78[76C7]	C7632	CAP_402	m78[76C2]	C7640	CAP_1206-1	m78[76D6]	C7641	CAP_1206-1	m78[76D6]	C7642	CAP_1206-1	m78[76D6]	C7643	CAP_1206-1	m78[76D6]	C7650	CAP_805	m78[76B7]	C7651	CAP_P_CASE-D3L	m78[76B8]	C7652	CAP_P_CASE-D3L	m78[76B8]	C7661	CAP_402	m78[76B3]	C7662	CAP_402	m78[76C4]	C7664	CAP_402	m78[76C3]	C7665	CAP_402	m78[76B4]	C7666	CAP_402	m78[76B3]	C7668	CAP_402	m78[76B2]	C7669	CAP_402	m78[76B2]	C7670	CAP_402	m78[76B4]	C7680	CAP_1206-1	m78[76D3]	C7681	CAP_1206-1	m78[76D4]	C7682	CAP_P_SM-1	m78[76D4]	C7689	CAP_402	m78[76B4]	C7690	CAP_805	m78[76B2]	C7691	CAP_P_CASE-D3L	m78[76B1]	C7692	CAP_P_CASE-D3L	m78[76B1]	C7693	CAP_P_CASE-D3L	m78[76B1]	C7700	CAP_805	m78[77C6]	C7701	CAP_402	m78[77C5]	C7702	CAP_402	m78[77B3]	C7705	CAP_805	m78[77B3]	C7706	CAP_805	m78[77B3]	C7707	CAP_805	m78[77B3]	C7710	CAP_805	m78[77D6]	C7712	CAP_402	m78[77D4]	C7715	CAP_805	m78[77D3]	C7800	CAP_402	m78[78D4]	C7801	CAP_402	m78[78D4]	C7810	CAP_402	m78[78D6]	C7811	CAP_402	m78[78D7]	C7850	CAP_402	m78[78C4]	C7851	CAP_402	m78[78C4]	C7890	CAP_805	m78[78D2]	C7891	CAP_402	m78[78D2]	C7895	CAP_402	m78[78B7]	C7896	CAP_402	m78[78A6]	C7899	CAP_402	m78[78B6]	C8400	CAP_P_SM-LF	m78[84C5]	C8401	CAP_805	m78[84C7]	C8420	CAP_402	m78[84C7]	C8421	CAP_402	m78[84C7]	C8422	CAP_402	m78[84C7]	C8423	CAP_402	m78[84C7]	C8424	CAP_402	m78[84B7]	C8425	CAP_402	m78[84B7]	C8426	CAP_402	m78[84B7]	C8427	CAP_402	m78[84B7]	C8428	CAP_402	m78[84B7]	C8429	CAP_402	m78[84B7]	C8430	CAP_402	m78[84B7]	C8431	CAP_402	m78[84B7]	C8432	CAP_402	m78[84B7]	C8433	CAP_402	m78[84B7]	C8434	CAP_402	m78[84B7]	C8435	CAP_402	m78[84B7]	C8436	CAP_402	m78[84B7]	C8437	CAP_402	m78[84B7]	C8438	CAP_402	m78[84B7]	C8439	CAP_402	m78[84B7]	C8440	CAP_402	m78[84B7]	C8441	CAP_402	m78[84A7]	C8442	CAP_402	m78[84A7]	C8443	CAP_402	m78[84A7]	C8444	CAP_402	m78[84A7]	C8445	CAP_402	m78[84A7]	C8446	CAP_402	m78[84A7]	C8447	CAP_402	m78[84A7]	C8448	CAP_402	m78[84A7]	C8449	CAP_402	m78[84A7]	C8450	CAP_402	m78[84A7]	C8451	CAP_402	m78[84A7]	C8500	CAP_805	m78[85A5]	C8570	CAP_402	m78[85D2]	C9000	CAP_603-1	m78[90C7]	C9001	CAP_402	m78[90C5]	C9010	CAP_402	m78[90A8]	C9020	CAP_1210	m78[90C5]	C9130	CAP_805	m78[91B7]	C9131	CAP_805-1	m78[91B7]	C9140	CAP_402	m78[91A5]	C9141	CAP_402	m78[91B5]	C9142	CAP_402	m78[91B5]	C9143	CAP_402	m78[91A6]	C9144	CAP_402	m78[91B6]	C9145	CAP_402	m78[91B6]	C9160	CAP_402	m78[91B4]	C9161	CAP_402	m78[91B4]	C9162	CAP_402	m78[91A2]	C9163	CAP_402	m78[91A2]	C9410	CAP_603	m78[94C9]	C9411	CAP_402	m78[94D3]	C9413	CAP_402	m78[94C2]	C9414	CAP_402	m78[94C2]	C9800	CAP_805	m78[98C5]	C9801	CAP_402	m78[98C4]	C9802	CAP_402	m78[98C4]	D2185	DIODE_SCHOT_SOT23	m78[21C4]	D2186	DIODE_SCHOT_SOT23	m78[21B4]	D2702	DIODE_SCHOT_6PB_SOT-363	m78[27D8 27D8]	D2800	DIODE_SCHOT_6PB_SOT-363	m78[28D6]	D4390	ZENER_SOT23	m78[43A6]	D4600	DIODE_SCHOT_3P_A_SC-	m78[46C2]	D4601	DIODE_SCHOT_3P_A_SC-	m78[46B5]	D4602	DIODE_SCHOT_3P_A_SC-	m78[46A5]	D5350	DIODE_3P_2NC_SOT23-L	m78[53C2]	D5600	DIODE_SOT23	m78[56C4]	D5601	DIODE_SOT23	m78[56B4]	D5700	DIODE_SOT23	m78[57C4]	D7100	DIODE_SCHOT_SMB	m78[71D2]	D7101	DIODE_SCHOT_SMB	m78[71B2]	D7200	DIODE_SCHOT_SMB	m78[72C3]	D7300	DIODE_SCHOT_5P_TLM83	m78[73B6]	D7301	DIODE_SCHOT_SOT23	m78[73C6]	D7373	DIODE_SCHOT_5P_TLM83	m78[73B3]	D7374	DIODE_SCHOT_SOT23	m78[73C3]	D7400	DIODE_SCHOT_5P_TLM83	m78[74B6]	D7401	DIODE_SCHOT_SOT23	m78[74C6]	D7473	DIODE_SCHOT_5P_TLM83	m78[74B3]	D7474	DIODE_SCHOT_SOT23	m78[74C4]	D7520	DIODE_SCHOT_5P_TLM83	m78[75C4]	D7600	DIODE_SCHOT_5P_TLM83	m78[76B7]	D7601	DIODE_SCHOT_5P_TLM83	m78[76B2]	D7624	DIODE_SCHOT_SOD-323	m78[76C6]	D7664	DIODE_SCHOT_SOD-323	m78[76C3]	D7810	DIODE_SCHOT_SOD-123	m78[78D7]	D7890	DIODE_SCHOT_SOD-123	m78[78D2]	D9400	ZENER_CASE425	m78[94C1]	D9410	DIODE_SCHOT_SOD-123	m78[94D6]	DE4300	DIODE_SCHOT_SOT	m78[43D7]	DP4310	DIODE_DUAL_6P_SOT-36	m78[43D4 43D3]	DP4311	DIODE_DUAL_6P_SOT-36	m78[43C4 43C3]	DP4320	DIODE_DUAL_6P_SOT-36	m78[43B5 43B4]	DP4321	DIODE_DUAL_6P_SOT-36	m78[43A5 43A4]	DS4599	LED_2_0X1.25MM-SM	m78[45C2]	F4300	FUSE_SM	m78[43D6]	F4310	FUSE_SM	m78[43D6]	F9410	FUSE_805	m78[94D5]	FL4300	FILTER_4P_L701-SM	m78[43B3]	FL4310	FILTER_4P_L701-SM	m78[43B3]	J600	CON_M12RT_D_THB_M-RT	m78[6D7]	J1000	MEROM_BGA-SKT-P	m78[10C3 10D7]	J1000	MEROM_BGA-SKT-P	m78[11D3 11D7]	J1300	CON_F60ST_D_SML_F-ST	m78[13C4]	J2800	BATTERY_2P_SM	m78[28D8]	J3100	CON_F200RT_DDR2DIMM	m78[31D5]	J3200	SMT_SM_F-RT-SM	m78[32D5]	J3400	CON_F52RT_D2MT_SM_F-	m78[34C5]	J3900	RT-SM	m78[39C3]	J4300	CON_F9ANG_1394B_D6MT	m78[43C2]	J4301	CON_F6ANG_S3MT_1394A	m78[43B2]	J4401	CON_M50ST_D2MT_SM1_M	m78[44C4]	J4510	CON_M7ST_SATA_SM_M-S	m78[45D7]	J4610	CON_F4ANG_S4MT_USB_T	m78[46D1]	J4620	CON_F4ANG_S4MT_USB_T	m78[46B4]	J4630	CON_F4ANG_S4MT_USB_T	m78[46A4]	J4700	CON_M5ST_S2MT_SM_M-S	m78[47B5]	J4720	CON_F10ST_D_SMA_F-ST	m78[47D2]	J5010	CON_M2ST_S2MT_SM_M-S	m78[50C6]	J5050	CON_M2ST_S2MT_SM_M-S	m78[50A3]	J5100	CON_F30STSM_S047_SM1	m78[51B5]	J5500	CON_M5ST_S2MT_SM_PN1	m78[55D7]	J5510	VD_M-ST-SM	m78[55A7]	J5511	CON_M2RT_S2MT_SM_M-R	m78[55A5]	J5550	CON_M3RT_S2MT_SM_M-R	m78[55B7]	J5551	CON_2RTSM_125_SM-2MT	m78[55B6]	J5560	CON_M5ST_S2MT_SM_PN1	m78[55D6]	J5600	CON_M4RT_S2MT_SM_M-R	m78[56D3]	J5601	CON_M4RT_S2MT_SM_M-R	m78[56B2]	J5700	CON_4SM_WRTB_85205-0	m78[57C2]	J5880	CON_M7ST_S2MT_SM_M-S	m78[58C6]	J8400	CON_F232RT_MXM_SM1_F	m78[85C6]	J9002	CON_F30ST_D_SM_F-ST-	m78[90B7]	J9410	CON_DVI_F32ST_Q2MT_S	m78[94D5]	J9800	M.F-ST-SM	m78[98C5]	L2150	IND_0603	m78[21A7]	L2173	IND_1210	m78[21D4]	L2181	IND_0603	m78[21D2]	L2183	IND_0603	m78[21C2]	L2190	IND_0805	m78[21B3]	L2195	IND_0805	m78[21A3]	L2700	IND_0805-1	m78[27C8]	L2702	IND_0805	m78[27A7]	L2703	IND_1210	m78[27A7]	L2901	IND_0402	m78[29D7]	L2902	IND_0402	m78[29D3]	L2903	IND_0402	m78[29C7]	L3800	IND_0805-1	m78[38D7]	L3810	IND_0805-1	m78[38B6]	L3900	IND_0805	m78[39D7]	L4200	IND_0402-LF	m78[42D5]	L4210	IND_0402-LF	m78[42B2]	L4211	IND_0402-LF	m78[42B2]	L4300	IND_SM	m78[43D3]	L4301	IND_SM	m78[43B4]	L4610	IND_SM	m78[46D3]	L4612	FILTER_4P_L701-SM	m78[46D3]	L4620	IND_SM	m78[46C6]	L4622	FILTER_4P_L701-SM	m78[46B6]	L4630	IND_SM	m78[46B6]	L4632	FILTER_4P_L701-SM	m78[46A6]	L4700	IND_SM	m78[47D6]	L4701	FILTER_4P_L701-SM	m78[47B6]	L4710	FILTER_4P_L701-SM	m78[47A6]	L5050	IND_3_8X3.8X1.5MM	m78[50A4]	L7100	IND_HM56-11120-TH	m78[71D2]	L7101	IND_HM56-11120-TH	m78[71B2]	L7200	IND_HM56-11120-TH	m78[72C3]	L7300	IND_MMD06EZ-SM	m78[73C7]	L7360	IND_MMD06EZ-SM	m78[73C2]	L7400	IND_MMD06EZ-SM	m78[74C7]	L7460	IND_IHLP5050-MMD12CE	m78[74C2]	L7580	IND_IHLP5050-MMD12CE	m78[75C3]	L7620	IND_MMD06EZ-SM	m78[76B7]	L7680	IND_HM56-11123-TH	m78[76B2]	L7700	IND_SM-MSS5131	m78[77B4]	L7710	IND_IHLP	m78[77D4]	L9000	IND_SM	m78[90C6]	L9140	IND_0402	m78[91A5]	L9141	IND_0402	m78[91B5]	L9142	IND_0402	m78[91B5]	L9160	IND_0402	m78[91B2]	L9161	IND_0402	m78[91A2]	L9400	FILTER_4P_SM	m78[94D7]	L9401	FILTER_4P_SM	m78[94D7]	L9402	FILTER_4P_SM	m78[94C7]	L9403	FILTER_4P_SM	m78[94B7]	L9410	IND_SM-1	m78[94B4]	LED601	LED_2_0X1.25MM-SM	m78[6A8]	LED602	LED_2_0X1.25MM-SM	m78[6A7]	LED603	LED_2_0X1.25MM-SM	m78[6A6]	LED604	LED_2_0X1.25MM-SM	m78[6B7]	LED3900	LED_2_0X1.25MM-SM	m78[39A7]	LED3901	LED_2_0X1.25MM-SM	m78[39A7]	LED3902	LED_2_0X1.25MM-SM	m78[39A7]	LED3903	LED_2_0X1.25MM-SM	m78[39A6]	LED4400	LED_2_0X1.25MM-SM	m78[44B5]	PP1000	

D	PP1442	PROBEPOINT_SM	m78[7C6]																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																					</
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D	R4950	RES_402	m78[49C4]	R7032	RES_402	m78[70C3]	R7630	RES_402	m78[76A7]	U2300	SB_ICH8M_BGA	m78[23D5]	C	B	A	R4951	RES_402	m78[49C4]	R7033	RES_402	m78[70C3]	R7631	RES_402	m78[76A7]	U2300	SB_ICH8M_BGA	m78[24B7 24D4]	A	A	A	A				
	R4998	RES_402	m78[49C2]	R7034	RES_402	m78[70D3]	R7661	RES_402	m78[76C2]	U2300	SB_ICH8M_BGA	m78[25D4]				R4999	RES_402	m78[49D4]	R7035	RES_402	m78[70B3]	R7664	RES_402	m78[76C3]	U2300	SB_ICH8M_BGA	m78[26D5 26D8]								
	R5000	RES_402	m78[50D6]	R7036	RES_402	m78[70B3]	R7665	RES_402	m78[76B4]	U2803	MC74VHC1G00_SC70-5	m78[28A7]				R5001	RES_402	m78[50C6]	R7037	RES_402	m78[70B3]	R7666	RES_402	m78[76C2]	U2900	CLK_SYN_SLG8LP537_QF	m78[29C5]								
	R5032	RES_402	m78[50B1]	R7038	RES_402	m78[70B3]	R7667	RES_402	m78[76B2]	U3700	88E8058_QFN	m78[37C4]				R5033	RES_402	m78[50B1]	R7039	RES_402	m78[70C3]	R7668	RES_402	m78[76B2]	U3780	EEPROM_M24C08_S08	m78[37B2]								
	R5034	RES_402	m78[50B1]	R7040	RES_402	m78[70C7]	R7669	RES_402	m78[76C2]	U4000	FW643_BGA	m78[40C5]				R5035	RES_402	m78[50B1]	R7041	RES_402	m78[70B7]	R7670	RES_402	m78[76C4]	U4600	SW1_TPS2060_MSOP	m78[46C7]								
	R5036	RES_402	m78[50B1]	R7060	RES_402	m78[70A7]	R7692	RES_402	m78[76A6]	U4601	SW1_TPS2068_MSOP	m78[46D7]				R5037	RES_402	m78[50B1]	R7061	RES_402	m78[70A6]	R7700	RES_402	m78[77C6]	U4650	PI3USB10_TDFN	m78[46D4]								
	R5038	RES_402	m78[50B1]	R7062	RES_402	m78[70A6]	R7701	RES_402	m78[77C5]	U4900	SMC_H8S2116_BGA	m78[49A3 49C3 49B7 49D7]				R5039	RES_402	m78[50B1]	R7063	RES_402	m78[70B6]	R7702	RES_402	m78[77B5]	U5000	VDET_RN5VD_SOT23-5A	m78[50D7]								
	R5040	RES_402	m78[50B1]	R7064	RES_402	m78[70B6]	R7703	RES_402	m78[77B3]	U5050	MM3120_LLP	m78[50A4]				R5041	RES_402	m78[50B1]	R7065	RES_402	m78[70C6]	R7704	RES_402	m78[77B3]	U5350	ZXCT1010_SOT23-5	m78[53C4]								
	R5042	RES_402	m78[50B1]	R7066	RES_402	m78[70C6]	R7705	RES_402	m78[77B2]	U5500	LM95214_LLP	m78[55B4]				R5043	RES_402	m78[50B1]	R7067	RES_402	m78[70C7]	R7710	RES_402	m78[77D6]	U5570	EMC1043_MSOP	m78[55D4]								
	R5046	RES_402	m78[50A1]	R7080	RES_402	m78[70D3]	R7711	RES_402	m78[77D6]	U6100	FLASH_SST25VF016B_SO	m78[61C5]				R5047	RES_402	m78[50B1]	R7081	RES_402	m78[70D3]	R7712	RES_402	m78[77D4]	U7010	COMPARATOR_LM339A_SO	m78[70D6]								
C	R5048	RES_402	m78[50A1]	R7092	RES_402	m78[70B3]	R7713	RES_402	m78[77C4]	U7052	MC74VHC1G08_SOT23-5-	m78[70C2]	B	A	A	R5050	RES_402	m78[50B6]	R7100	RES_402	m78[71C2]	R7800	RES_402	m78[78D5]	U7100	ISL6260C_QFN	m78[71C6]	A	A	A	A				
	R5051	RES_402	m78[50B7]	R7101	RES_603	m78[71C2]	R7801	RES_402	m78[78D5]	U7101	ISL6208_QFN	m78[71D5]				R5052	RES_402	m78[50A7]	R7102	RES_1206	m78[71B3]	R7810	RES_402	m78[78D8]	U7201	ISL6208_QFN	m78[72C7]								
	R5052	RES_402	m78[50A7]	R7102	RES_1206	m78[71B3]	R7811	RES_402	m78[78D7]	U7300	ISL6539_SSOP	m78[73C5]				R5053	RES_402	m78[50A6]	R7103	RES_1206	m78[71D3]	R7811	RES_402	m78[78D7]	U7400	ISL6539_SSOP	m78[74C5]								
	R5055	RES_402	m78[50A3]	R7103	RES_1206	m78[71D3]	R7851	RES_402	m78[78C5]	U7500	ISL6269_QFN	m78[75D6]				R5056	RES_402	m78[50A3]	R7104	RES_402	m78[71C1]	R7850	RES_402	m78[78C5]	U7501	SN74LVC1G07_SC70	m78[75D8]								
	R5056	RES_402	m78[50A3]	R7105	RES_402	m78[71B2]	R7851	RES_402	m78[78C5]	U7550	LREQ_BD3533FVM_MSOP-	m78[75B4]				R5057	RES_402	m78[50A6]	R7106	RES_603	m78[71B2]	R7870	RES_402	m78[78B7]	U7600	LM339A_SO	m78[76C5]								
	R5058	RES_402	m78[50A5]	R7107	RES_402	m78[71B1]	R7871	RES_402	m78[78B7]	U7601	COMPARATOR_LM393_SOI	m78[76D6 76A7]				R5059	RES_402	m78[50A4]	R7107	RES_402	m78[71B1]	R7871	RES_402	m78[78B7]	U7710	TPS62050_MSOP	m78[77D5]								
	R5070	RES_402	m78[50D2]	R7108	RES_402	m78[71C8]	R7888	RES_402	m78[78C1]	U7750	TPS62510_BQA	m78[77B4]				R5071	RES_402	m78[50D3]	R7109	RES_402	m78[71B7]	R7889	RES_402	m78[78C2]	U8500	RES_402	m78[85C7]								
	R5078	RES_402	m78[50D1]	R7111	RES_402	m78[71B8]	R7892	RES_402	m78[78D2]	U8501	RES_402	m78[85C5]				R5080	RES_402	m78[50D1]	R7112	RES_402	m78[71D7]	R7892	RES_402	m78[78D2]	U8570	EEPROM_M24C02_S08	m78[85D2]								
	R5080	RES_402	m78[50B1]	R7112	RES_402	m78[71D7]	R7893	RES_402	m78[78D3]	U9130	VIDEO_TS3V330_SOP	m78[91B7]				R5087	RES_402	m78[50B1]	R7113	RES_402	m78[71D7]	R7894	RES_805	m78[78D1]	U9160	74LVC1G125LF_SOT23-5	m78[91B4]								
	R5082	RES_402	m78[50B1]	R7114	RES_402	m78[71B7]	R7894	RES_805	m78[78D1]	U9161	74LVC1G125LF_SOT23-5	m78[91A4]				R5088	RES_402	m78[50A1]	R7115	RES_402	m78[71C8]	R7895	RES_402	m78[78A7]	U9501	VR5900	m78[95C2]								
B	R5083	RES_402	m78[50A1]	R7115	RES_402	m78[71B4]	R7895	RES_402	m78[78A7]	U9501	VR5900	m78[95C2]	A	A	A	R5084	RES_402	m78[50A1]	R7116	RES_402	m78[71B4]	R7896	RES_402	m78[78A6]	U9501	VR5900	m78[95C2]					A	A	A	A
	R5086	RES_402	m78[50A1]	R7117	RES_402	m78[71B5]	R7897	RES_402	m78[78B6]	U9501	VR5900	m78[95C2]				R5087	RES_402	m78[50A1]	R7118	RES_402	m78[71B5]	R7898	RES_402	m78[78B6]	U9501	VR5900	m78[95C2]								
	R5088	RES_402	m78[50A1]	R7119	RES_402	m78[71C8]	R7898	RES_402	m78[78B6]	U9501	VR5900	m78[95C2]				R5090	RES_402	m78[50A1]	R7120	RES_402	m78[71D7]	R7899	RES_402	m78[78B6]	U9501	VR5900	m78[95C2]								
	R5090	RES_402	m78[50B1]	R7120	RES_402	m78[71D7]	R8500	RES_402	m78[85C7]	U9501	VR5900	m78[95C2]				R5091	RES_402	m78[50B1]	R7121	RES_402	m78[71D7]	R8501	RES_402	m78[85C5]	U9501	VR5900	m78[95C2]								
	R5092	RES_402	m78[50B1]	R7122	RES_402	m78[71A4]	R8502	RES_402	m78[85C7]	U9501	VR5900	m78[95C2]				R5093	RES_402	m78[50B1]	R7122	RES_402	m78[71A4]	R8503	RES_402	m78[85A4]	U9501	VR5900	m78[95C2]								
	R5093	RES_402	m78[50B1]	R7123	RES_402	m78[71A4]	R8505	RES_402	m78[85B4]	U9501	VR5900	m78[95C2]				R5094	RES_402	m78[50B1]	R7123	RES_402	m78[71A4]	R8505	RES_402	m78[85B4]	U9501	VR5900	m78[95C2]								
	R5094	RES_402	m78[50B1]	R7126	RES_402	m78[71C8]	R8570	RES_402	m78[85D3]	U9501	VR5900	m78[95C2]				R5096	RES_402	m78[50B1]	R7126	RES_402	m78[71C8]	R8570	RES_402	m78[85D3]	U9501	VR5900	m78[95C2]								
	R5096	RES_402	m78[50B1]	R7127	RES_402	m78[71C7]	R9000	RES_402	m78[90C8]	U9501	VR5900	m78[95C2]				R5099	RES_402	m78[50B1]	R7127	RES_402	m78[71C7]	R9000	RES_402	m78[90C8]	U9501	VR5900	m78[95C2]								
	R5190	RES_402	m78[51B2]	R7130	RES_402	m78[71B4]	R9001	RES_402	m78[90C7]	U9501	VR5900	m78[95C2]				R5191	RES_402	m78[51C3]	R7131	RES_402	m78[71B4]	R9002	RES_805	m78[90C8]	U9501	VR5900	m78[95C2]								
	R5192	RES_402	m78[51C4]	R7140	RES_603	m78[71B1]	R9003	RES_805	m78[90C8]	U9501	VR5900	m78[95C2]				R5192	RES_402	m78[51C4]	R7140	RES_603	m78[71B1]	R9003	RES_805	m78[90C8]	U9501	VR5900	m78[95C2]								
A	R5200	RES_402	m78[52D7]	R7141	RES_603	m78[71C1]	R9070	RES_402	m78[90B7]	U9501	VR5900	m78[95C2]	A	A	A	R5201	RES_402	m78[52D7]	R7142	RES_402	m78[71D4]	R9070	RES_402	m78[90B7]	U9501	VR5900	m78[95C2]					A	A	A	A
	R5230	RES_402	m78[52A7]	R7143	RES_402	m78[71C4]	R9071	RES_402	m78[90B2]	U9501	VR5900	m78[95C2]				R5231	RES_402	m78[52A7]	R7143	RES_402	m78[71C4]	R9075	RES_402	m78[90B2]	U9501	VR5900	m78[95C2]								
	R5231	RES_402	m78[52A7]	R7197	RES_402	m78[71D6]	R9090	RES_805	m78[90C6]	U9501	VR5900	m78[95C2]				R5250	RES_402	m78[52D4]	R7199	RES_402	m78[71C7]	R9099	RES_402	m78[90C8]	U9501	VR5900	m78[95C2]								
	R5250	RES_402	m78[52D4]	R7199	RES_402	m78[71C7]	R9099	RES_402	m78[90C8]	U9501	VR59																								