

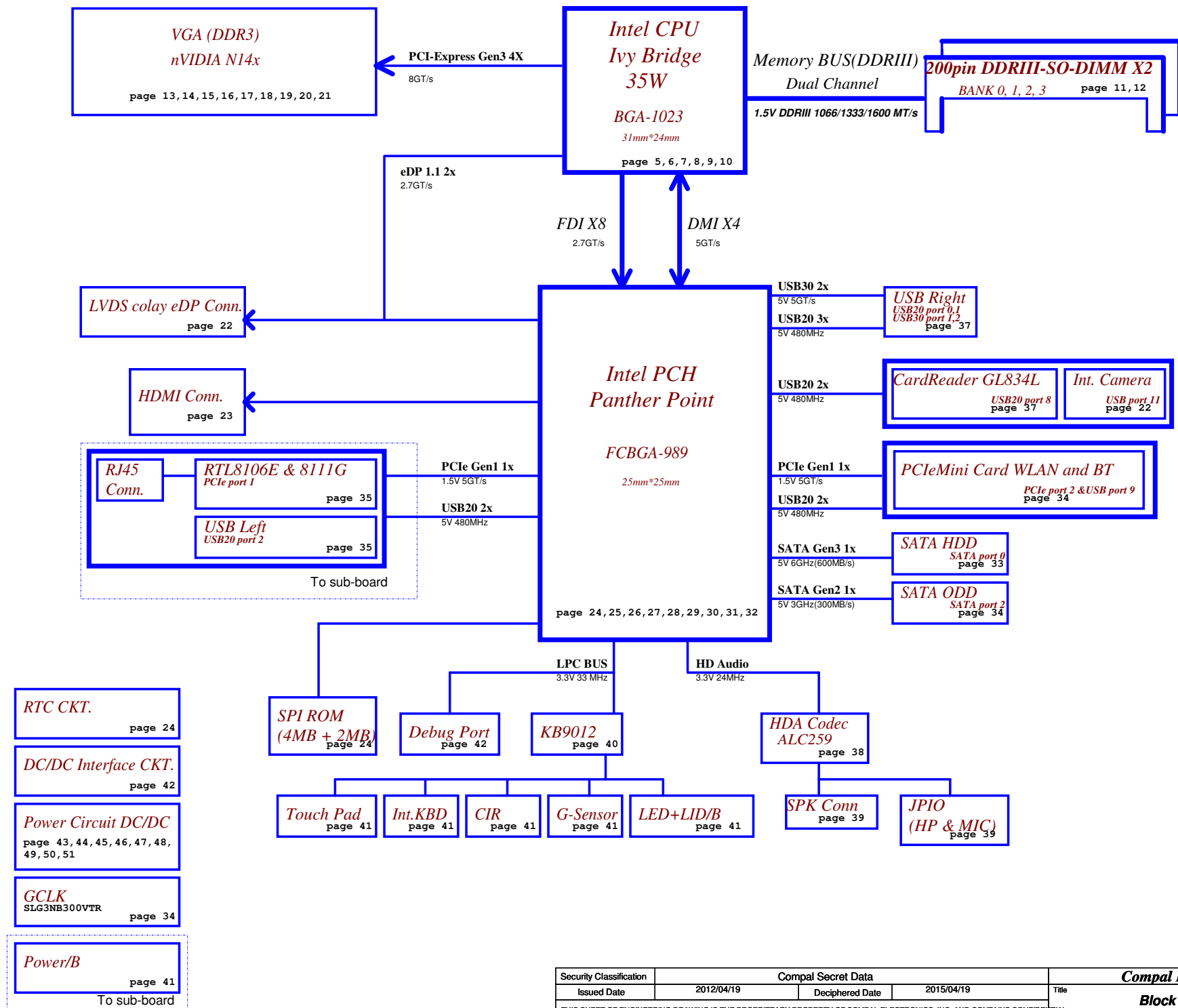
VFKTA

Rosetta 10FT/10FTG

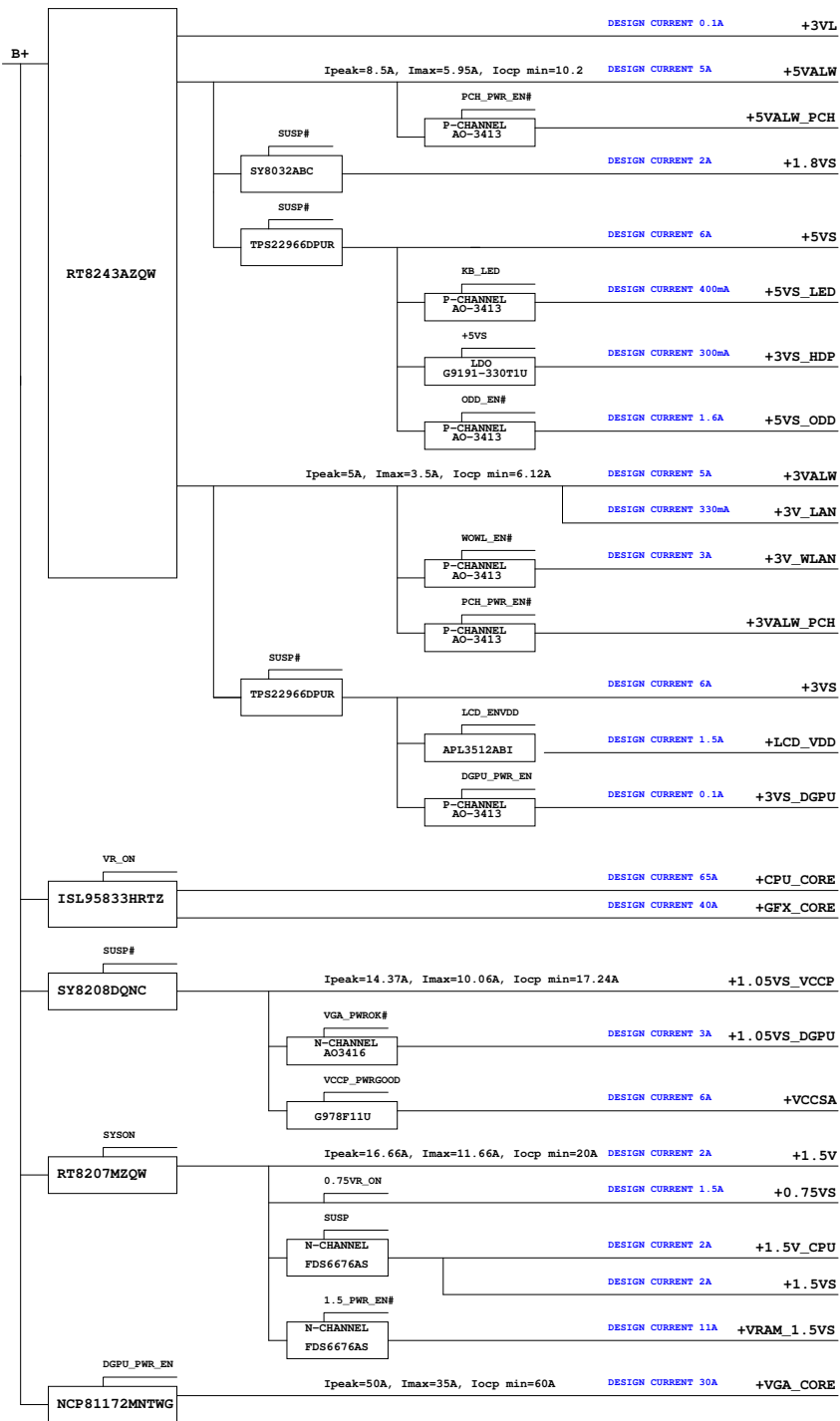
LA-9861P REV 0.3 Schematic

Intel Processor (Ivy Bridge/Sandy Bridge)+
PCH(Panther Point)
2013-01-11 Rev 0.3

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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	Cover Page
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				VFKTA	0.3
Date: Thursday, January 17, 2013				Sheet	1 of 56



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								Block Diagram	
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						VFKTA		0.3	
						Date		Thursday, January 17, 2013	
						Sheet		2 of 56	



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Date	Thursday, January 17, 2013	ISheet	3	of	81

Voltage Rails

(O MEANS ON X MEANS OFF)

<div>power plane</div> <div>State</div>	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	WLAN/WIMAX		

EC SM Bus1 Address

EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b	+3VS	NVIDIA GPU	9E H	1001 1010 b
+3VL	USB S&C 14640	35 H	0011 0101 b	+3VS	G-Sensor	40 H	0100 0000 b

BTO Option Table

Function	CPU	
description	Ivy Bridge i3	Ivy Bridge i5
explain	Ivy Bridge i3	Ivy Bridge i5
BTO	CPUI3@	CPUI5@

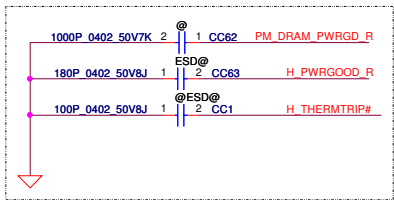
Function	WOWL	G-SENSOR	ZPODD		LVDS-eDP		Camera & Mic			KB Light
description	WOWL	G-SENSOR	ZPODD		LVDS-eDP		Camera & Mic			KB Light
explain	WOWL	G-SENSOR	w/	w/o	LVDS	eDP	Camera & Mic			KB Light
BTO	WOWL@	GSSENSOR@	ZPODD@	NONZF@	LVDS@	IEDP@	CAM@	CAM@EMI@	@CAM@EMI@	KBL@

Function	GPU		GCLK			PCH		VRAM
description	N14M-GL	N14P-GV2	GCLK			non-GCLK		Panther Point
explain	N14M-GL	N14P-GV2	GCLK			non-GCLK		HM76 HM70
BTO	N14MGL@	N14PGV2@	GCLK@	GCLK@EMI@	@GCLK@EMI@	NOGCLK@		HM76R1@ HM70R1@ DRANK@

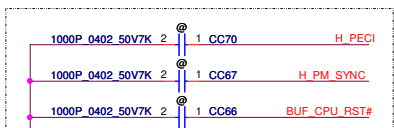
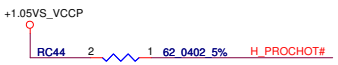
Function	EMI/ESD/RF part			Sleep & Music		CRT		Touch Screen
description	EMI/ESD/RF part			Sleep & Music		CRT		Touch Screen
explain	EMI/ESD/RF part			w/ S&M	w/o S&M	w/ CRT		w/o CRT
BTO	EMI@	@EMI@	ESD@	@ESD@	@RF@	269@	259@	CRT@ CRT@EMI@ NOCRT@ TOUCH@EMI@

Function	EC		ISPD	
description	EC		HDMI Logo	
explain	KB9012	NPCE885N	HDMI Logo	
BTO	9012@	885@	HDMI45@	

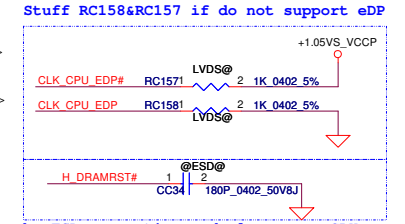
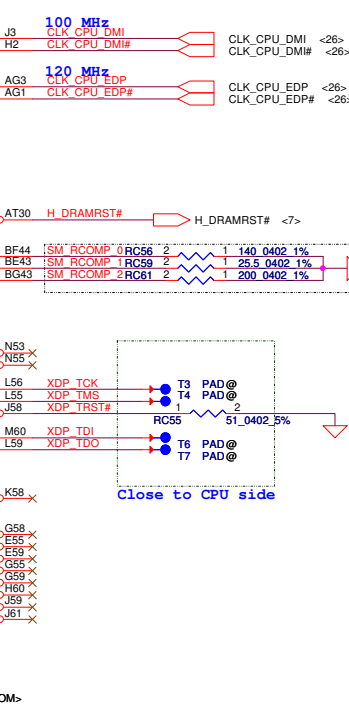
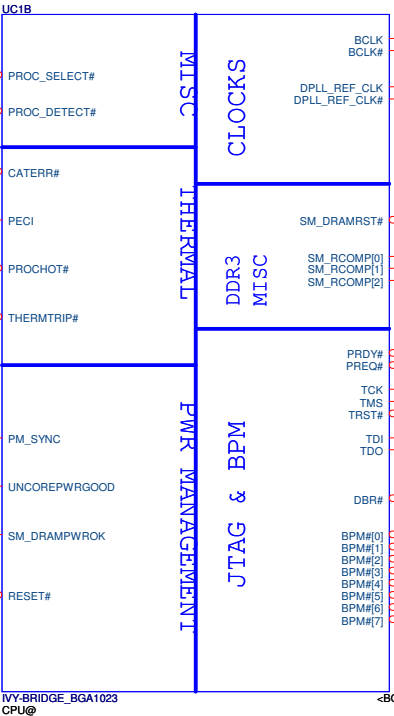
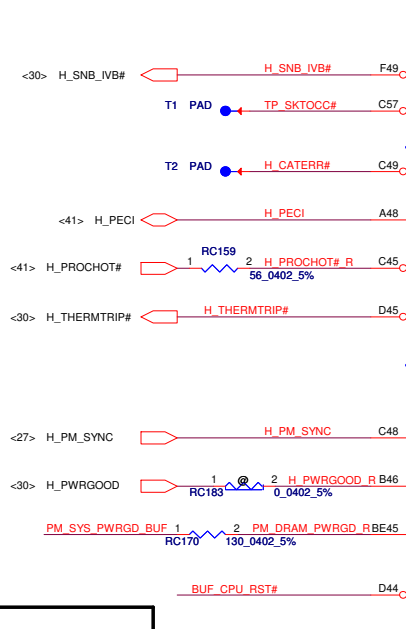
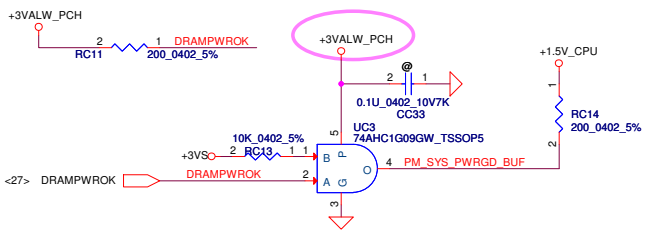
Red Word: don't mount



by ESD request and place near CPU

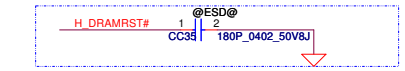


Please place near JCPU



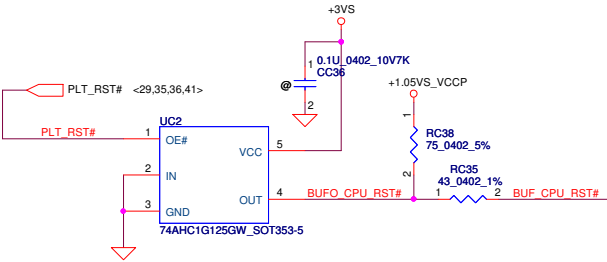
by ESD request and place near CPU

DDR3 Compensation Signals
Layout Note: Place these resistors near Processor



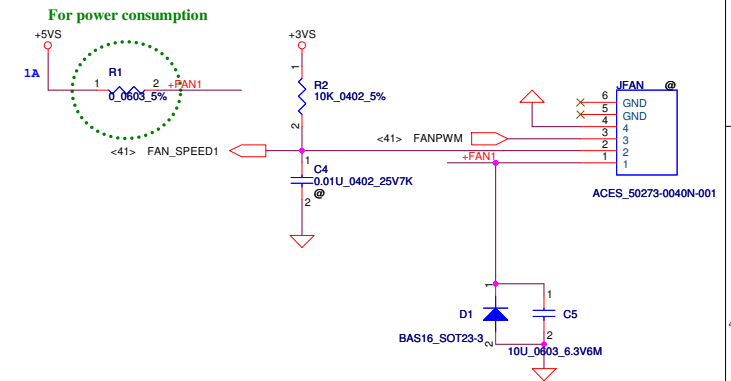
Routed as a single daisy chain

Buffered Rest to CPU

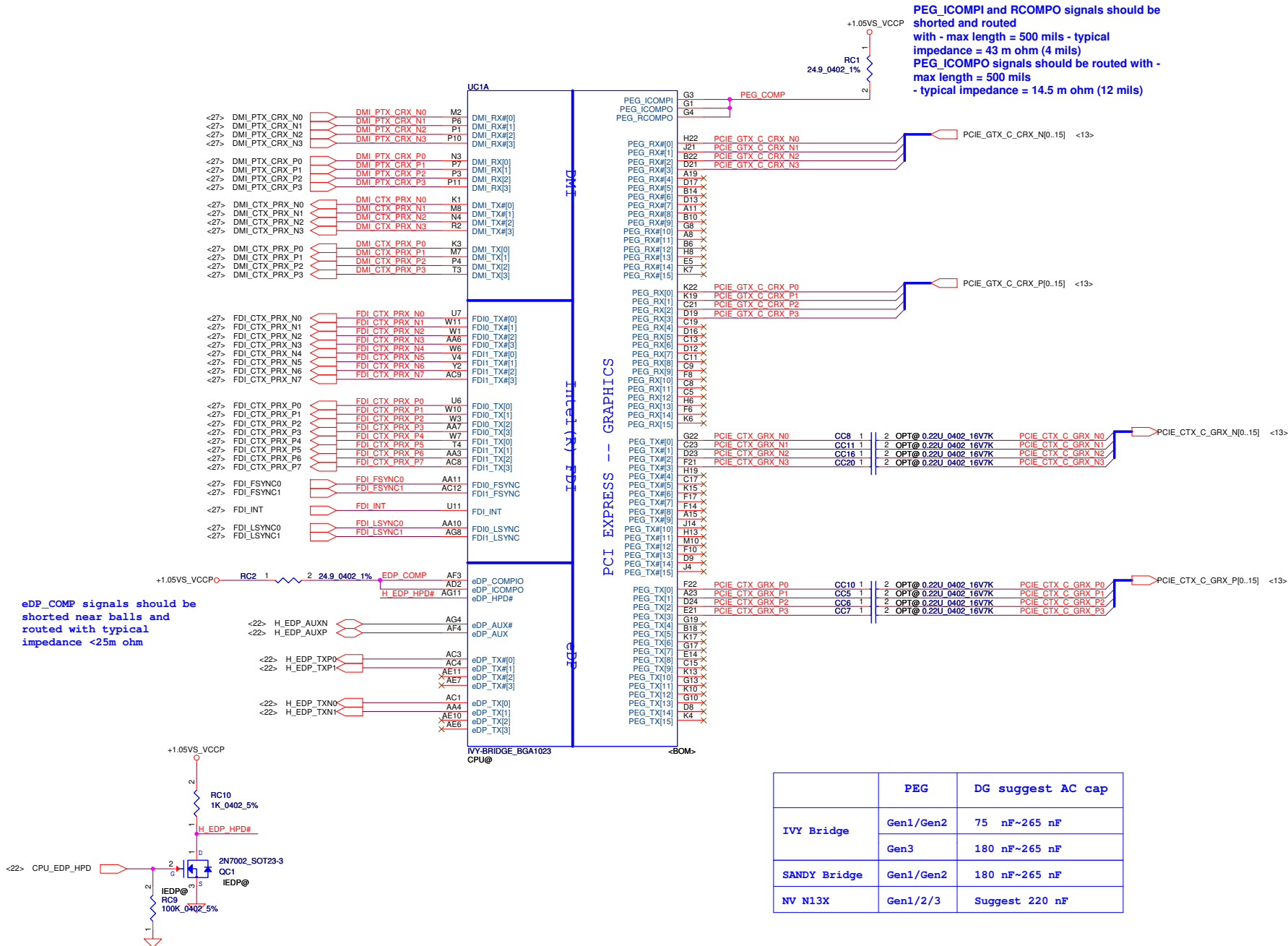


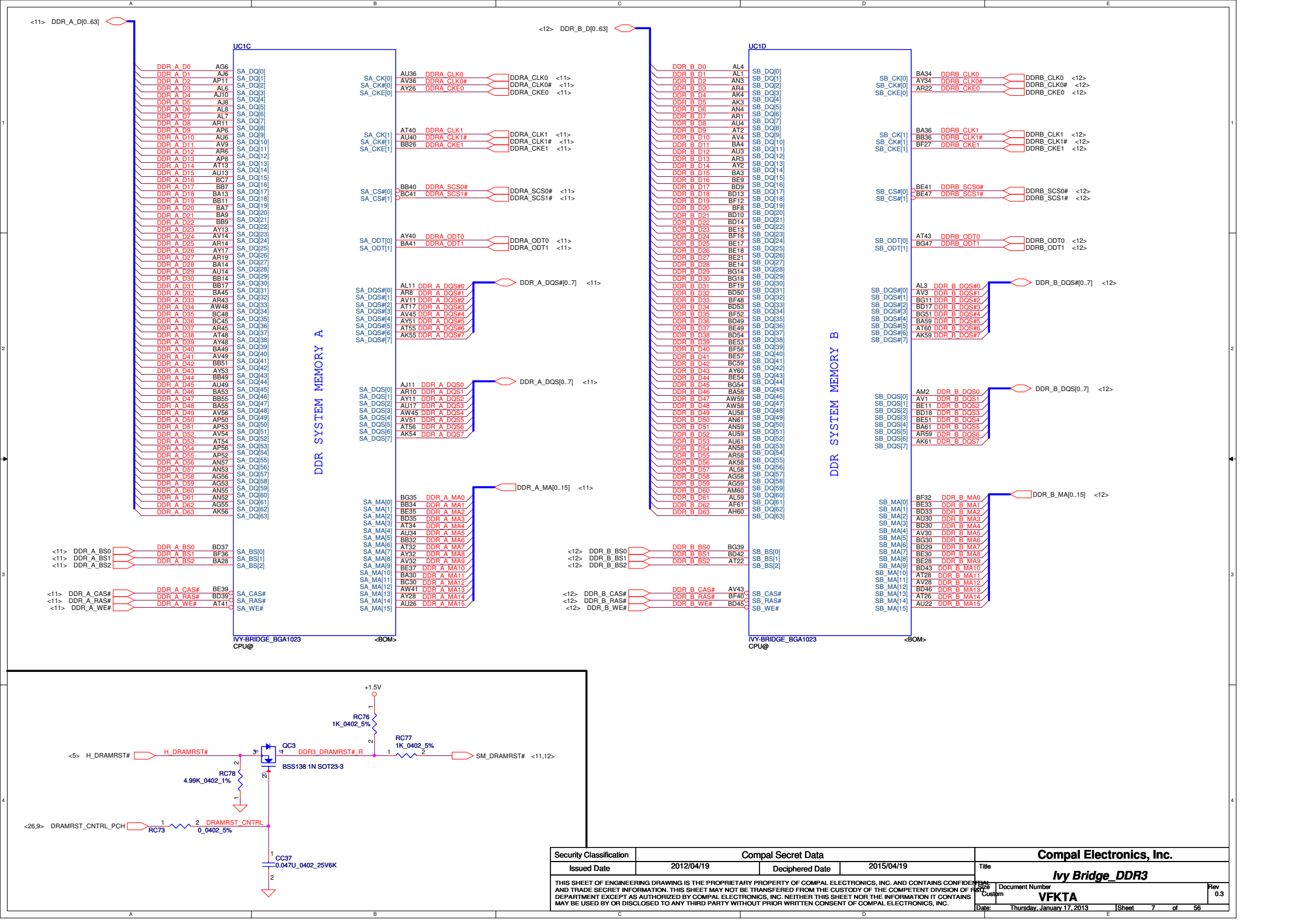
XDP Connector

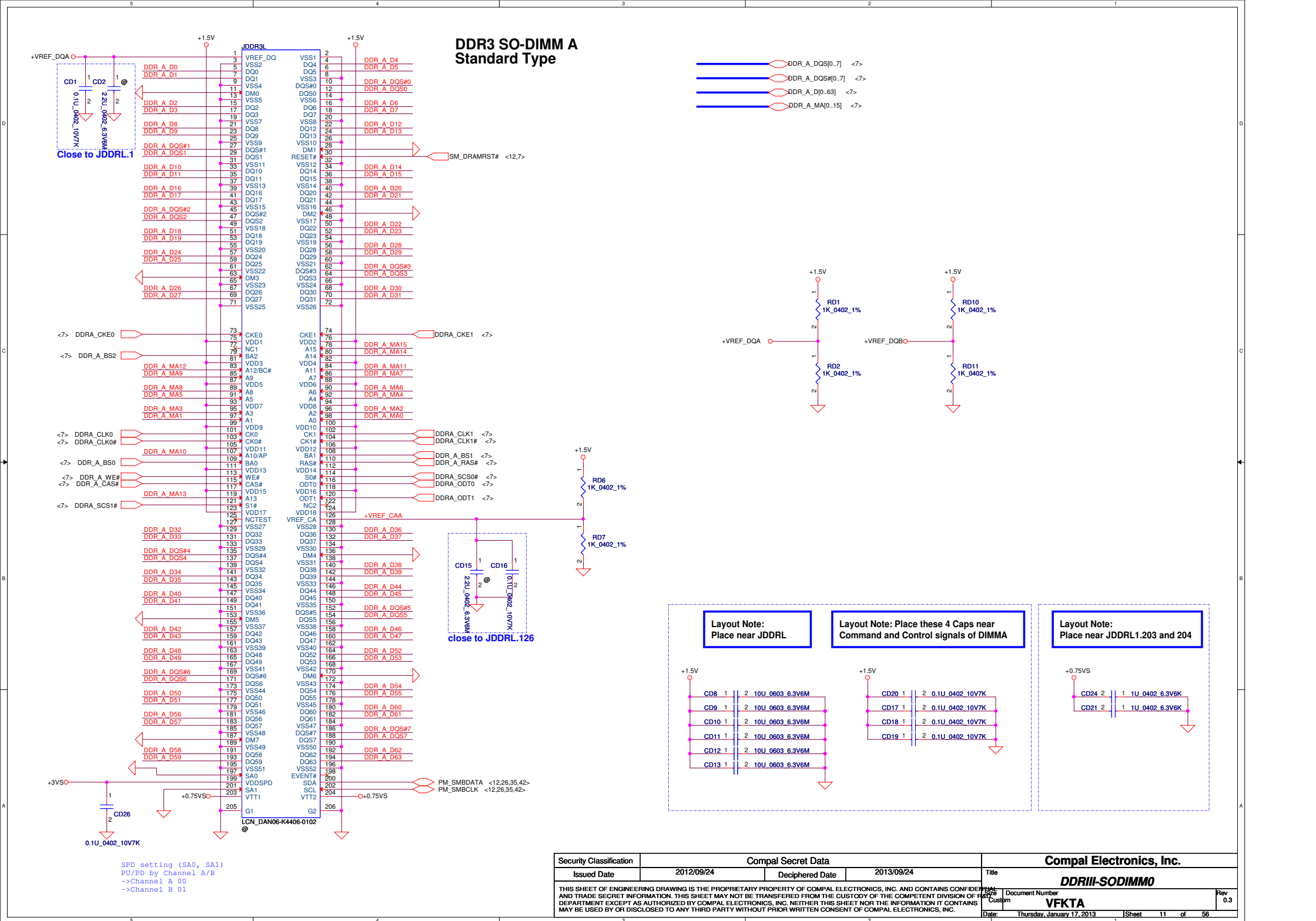
FAN Control Circuit

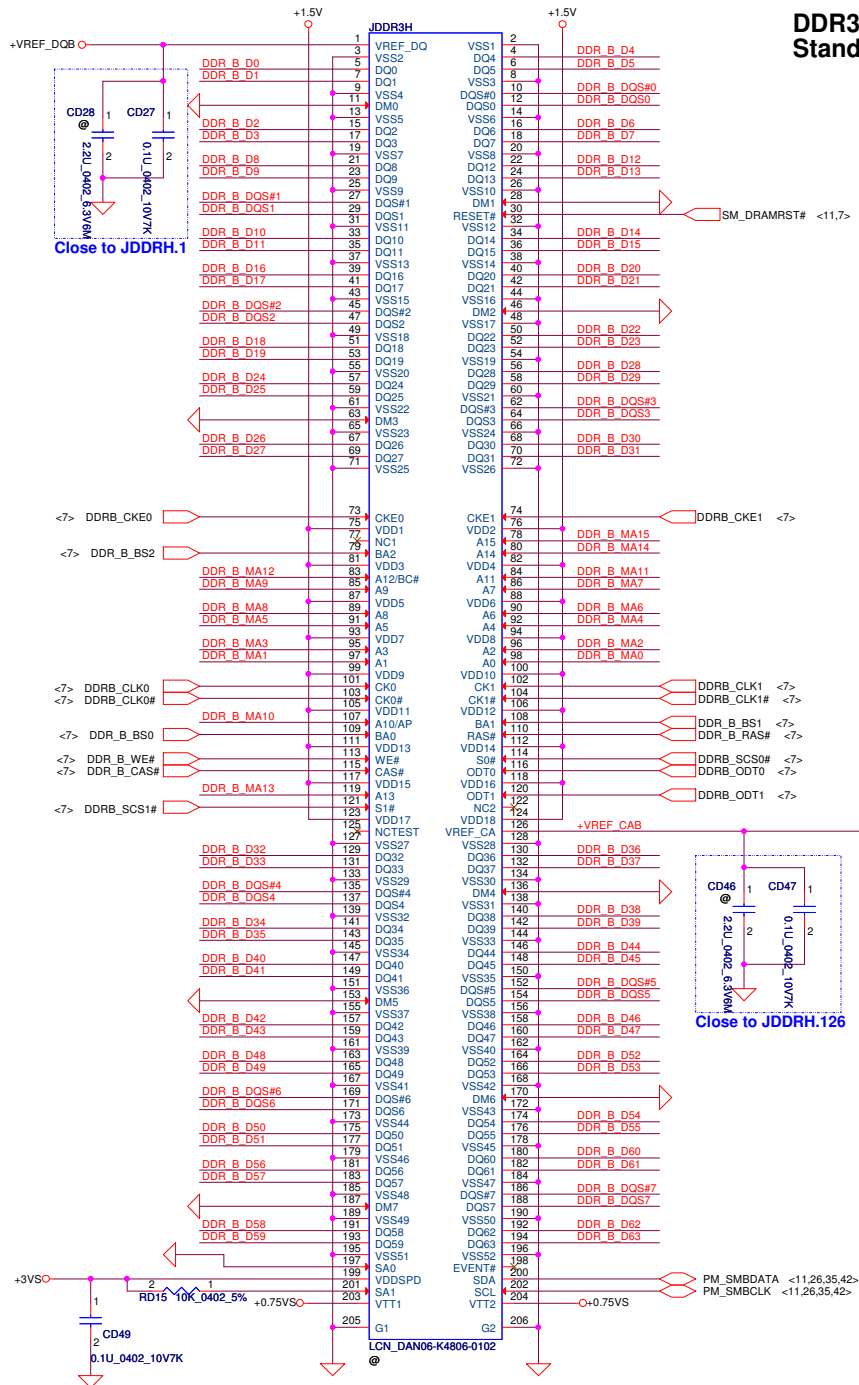


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Ivy Bridge_JTAG/XDP/FAN				
VFKTA				
Date: Thursday, January 17, 2013				
Sheet 5 of 56				



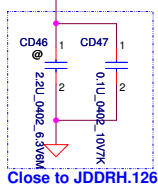






DDR3 SO-DIMM B Standard Type

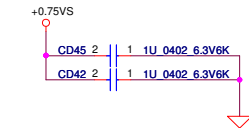
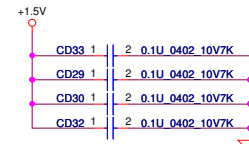
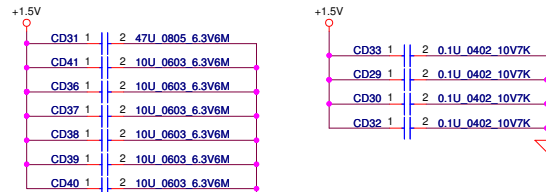
DDR_B_DQS#0[0..7] <7>
DDR_B_DQS#0[0..7] <7>
DDR_B_D[0..63] <7>
DDR_B_MA[0..15] <7>



Layout Note:
Place near JDDRH

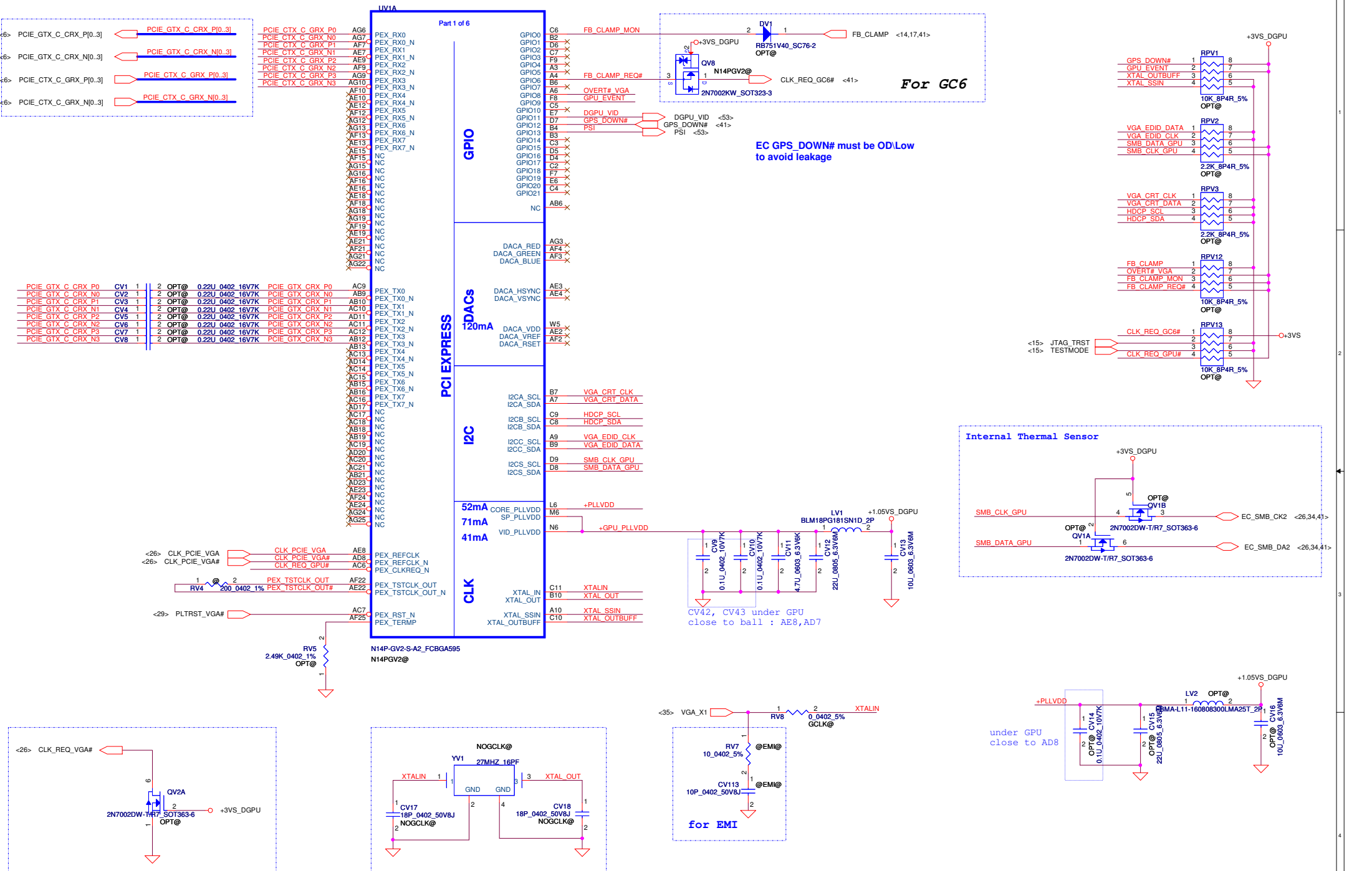
Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB

Layout Note:
Place near JDDRH.203 and 204

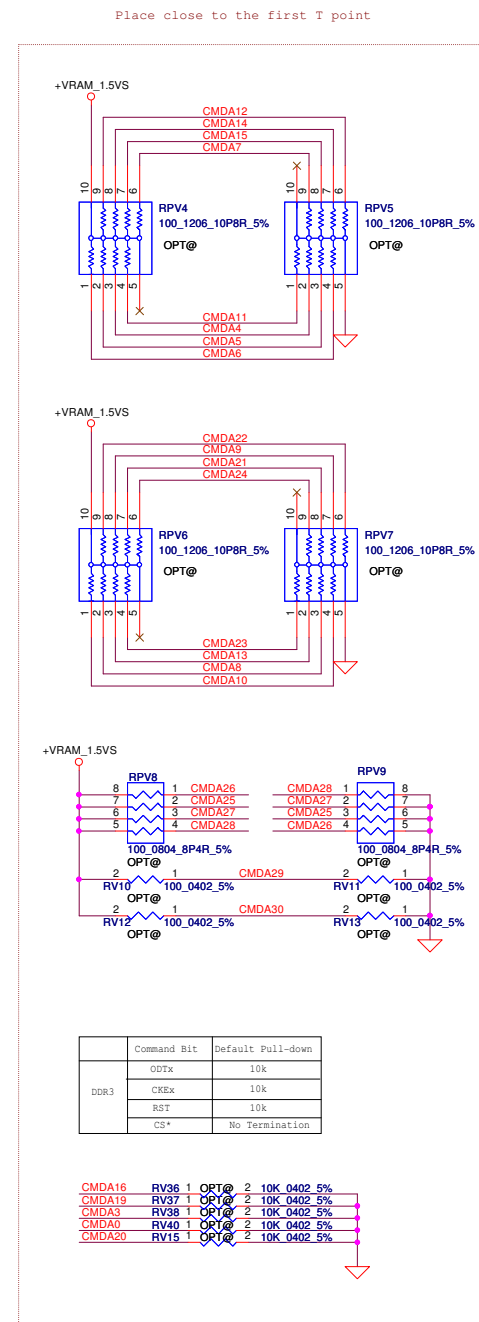
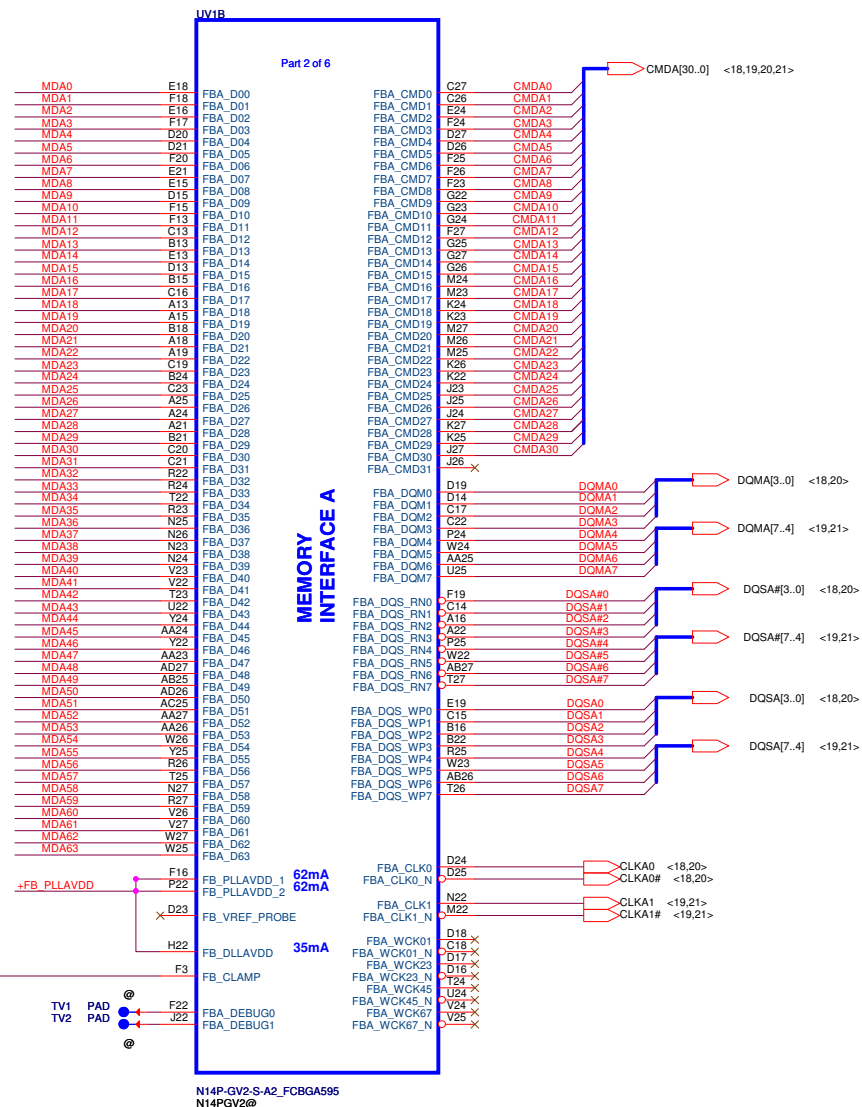


SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

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				Date	Thursday, January 17, 2013
				Sheet	12 of 56

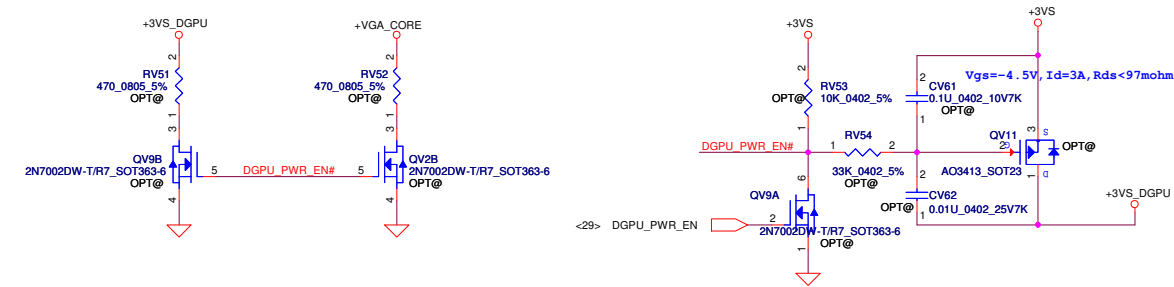
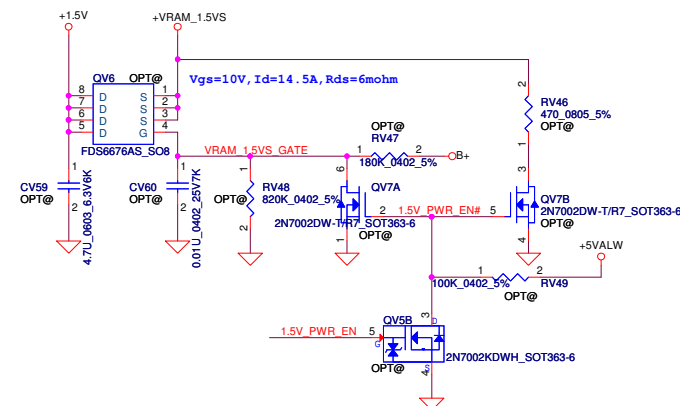
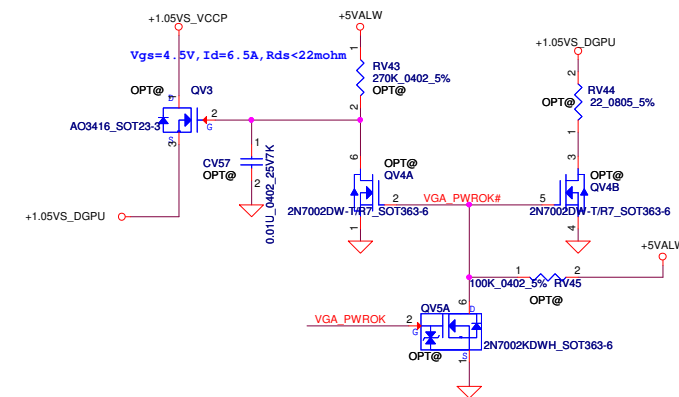
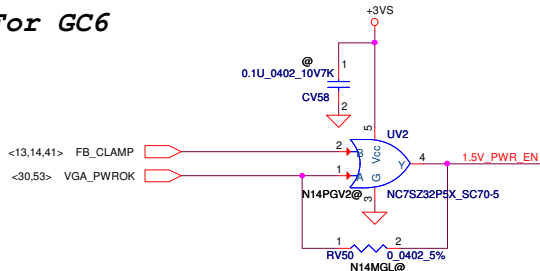


VRAM Interface



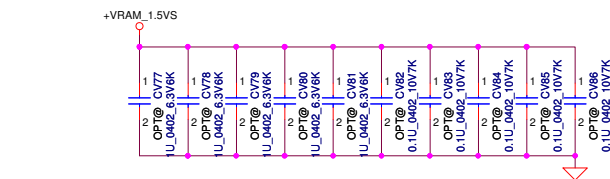
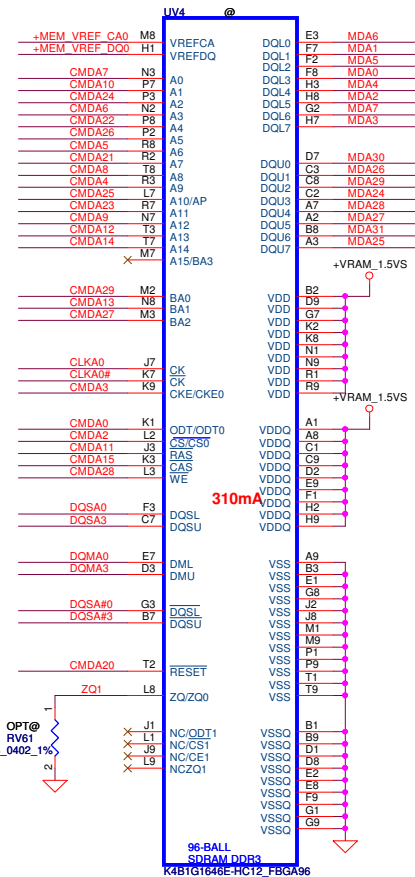
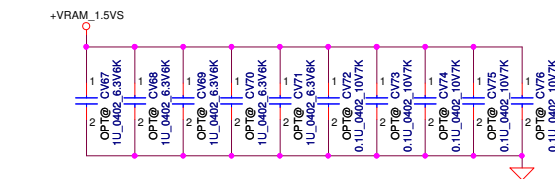
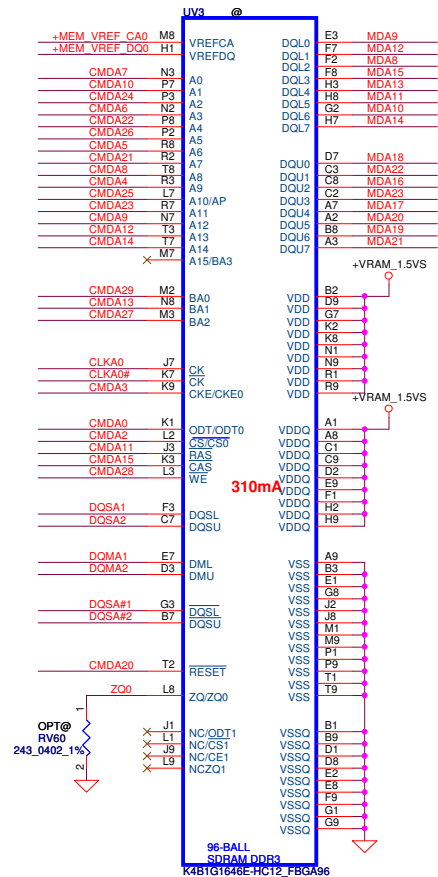
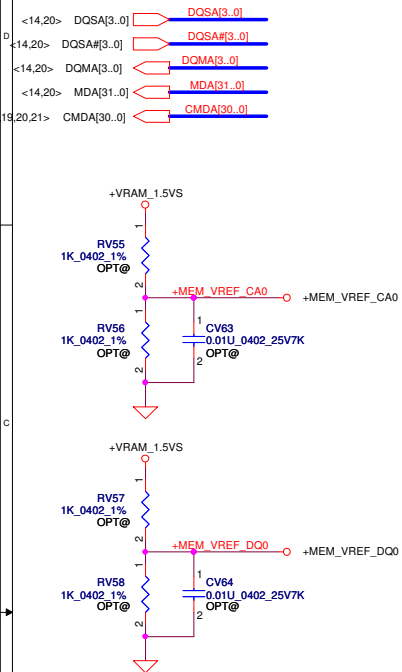
	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

CMDA16	RV36	1	OPT@	2	10K	0402	5%
CMDA19	RV37	1	OPT@	2	10K	0402	5%
CMDA3	RV38	1	OPT@	2	10K	0402	5%
CMDA0	RV40	1	OPT@	2	10K	0402	5%
CMDA20	RV15	1	OPT@	2	10K	0402	5%

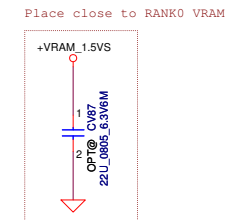
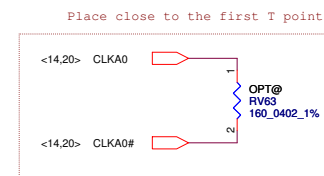


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				Date: Thursday, January 17, 2013	Sheet 17 of 56

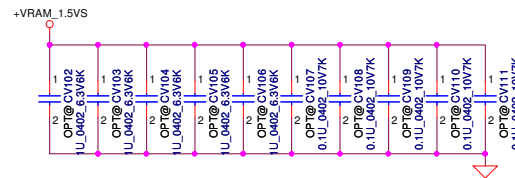
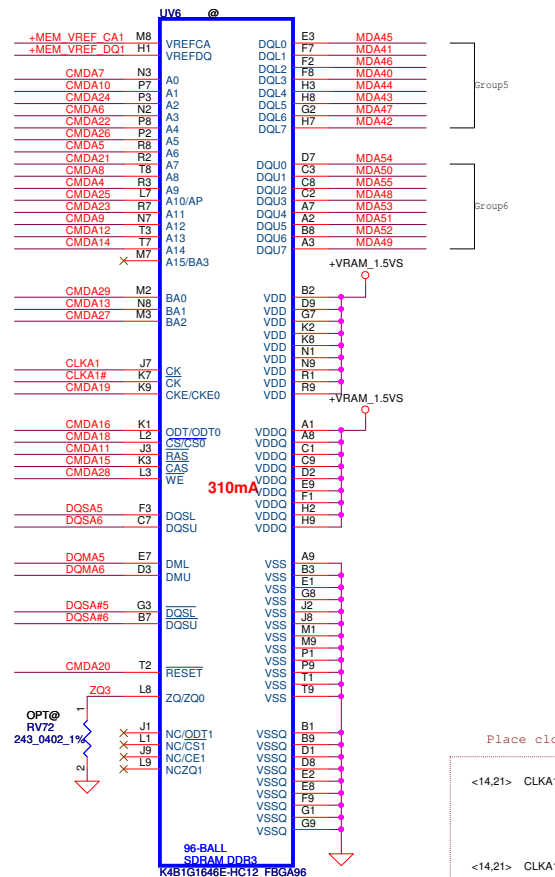
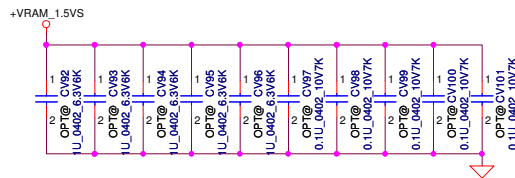
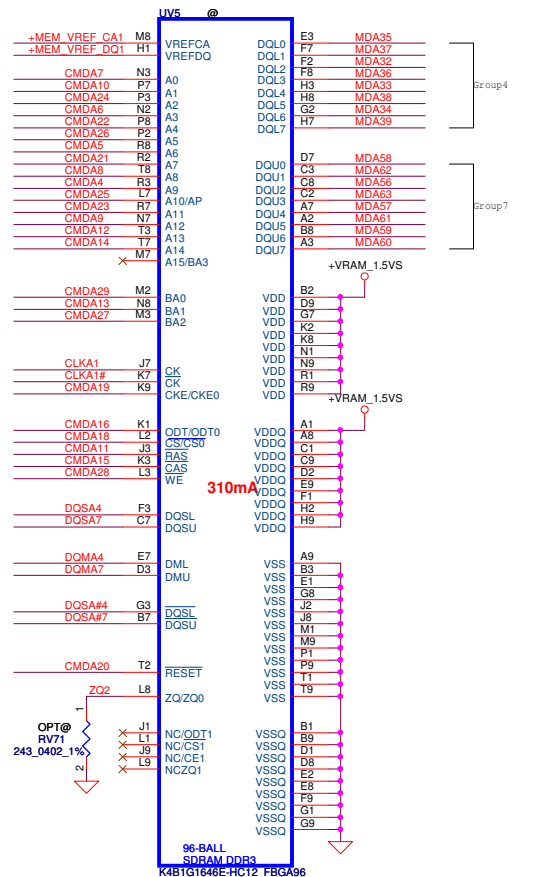
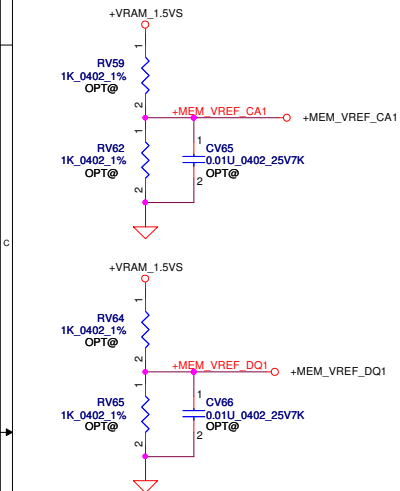
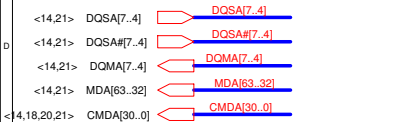
VRAM DDR3 Chips



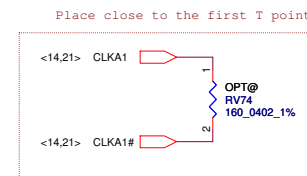
Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2



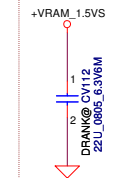
RANK 0 [63...32] VRAM DDR3 Chips



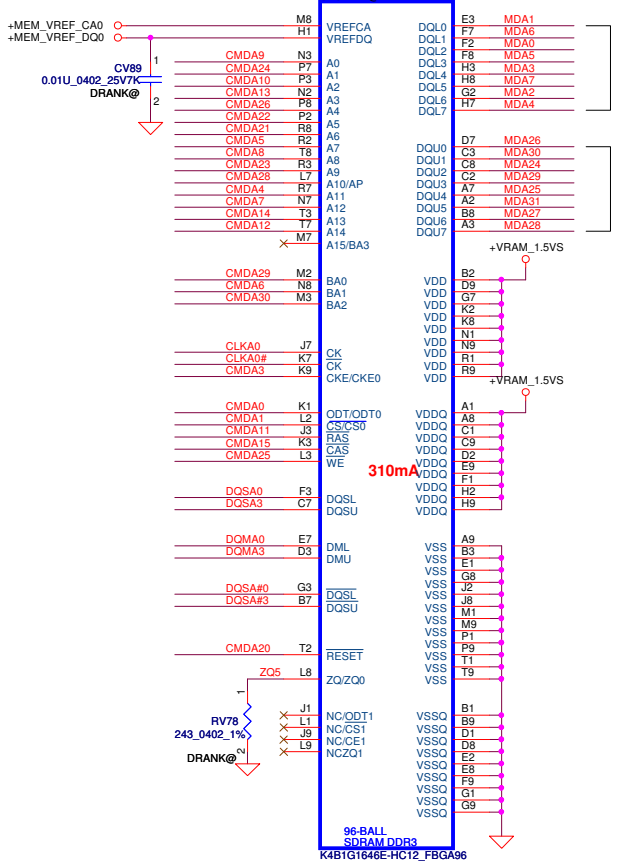
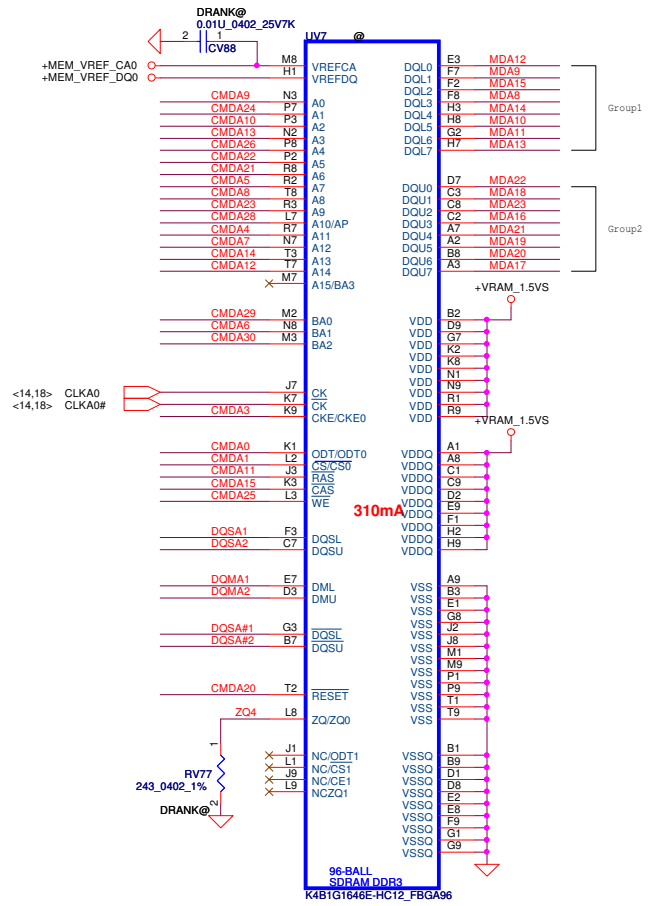
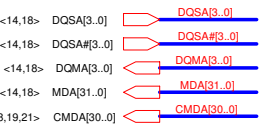
Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17			CS1#	
CMD18		CS0#		
CMD19		CKE	CKE	
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2



Place close to RANK1 VRAM



RANK 1 [31...0]
VRAM DDR3 Chips



Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17			CS1#	
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

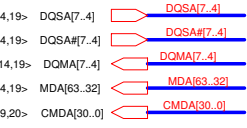
4,19> DQSA[7..4] → DQSA[7..4]

4,19> DQSA#[7..4] → DQSA#[7..4]

14,19> DQMA[7..4] → DQMA[7..4]

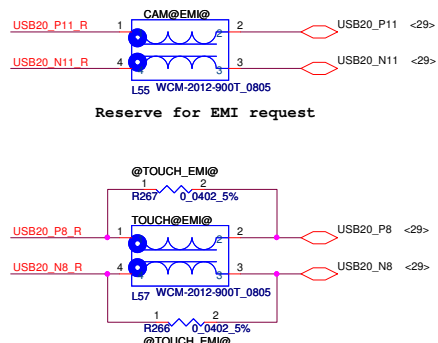
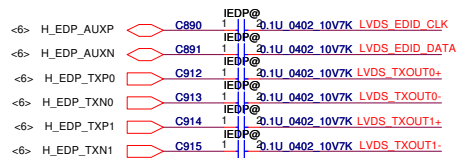
4,19> MDA[63..32] → MDA[63..32]

9,20> CMDA[30..0] → CMDA[30..0]



CMD3	A9	A9	A11	A11
CMD4	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8

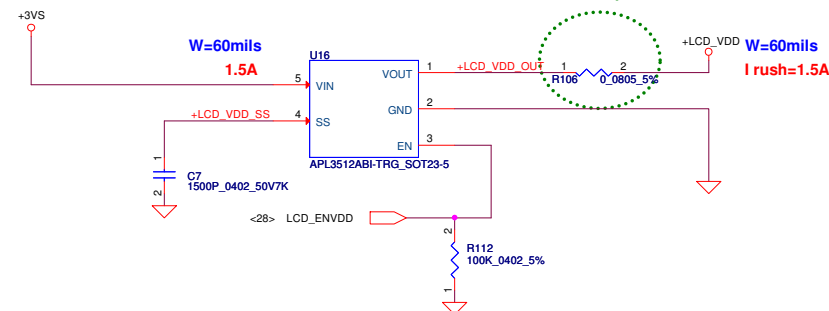
For eDP Panel



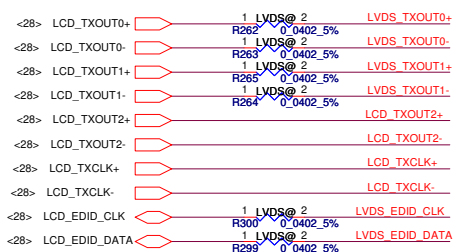
LCD POWER CIRCUIT

Need check eDP&LVDS both 3V power rail.

Reserve for power consumption
Remove on PVT phase



For LVDS 1ch Panel



Reserve for EMI request

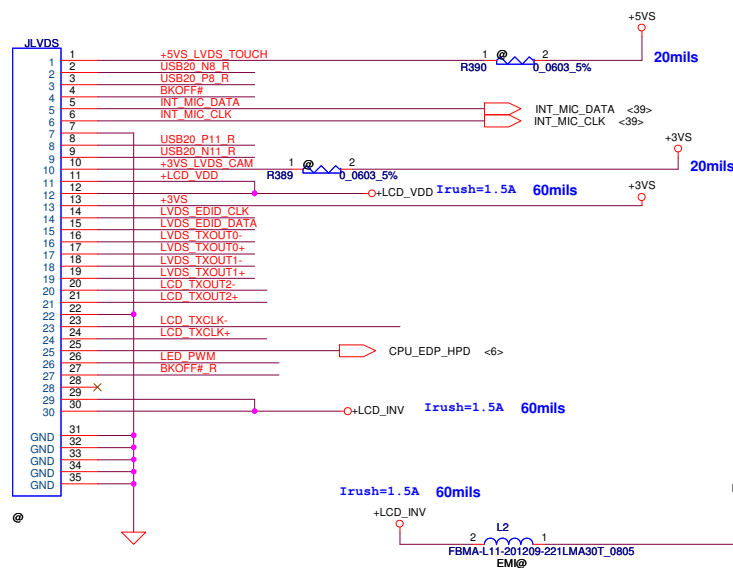
LVDS colay eDP cable

Pin define will be change after ME ready

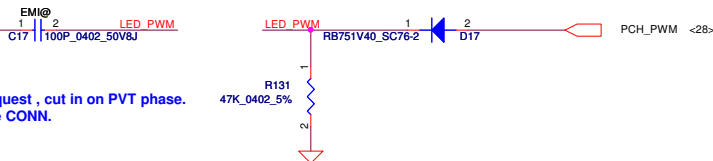
pin1-4 Touch function for panel

pin5-10 For Webcam with single or dual MIC

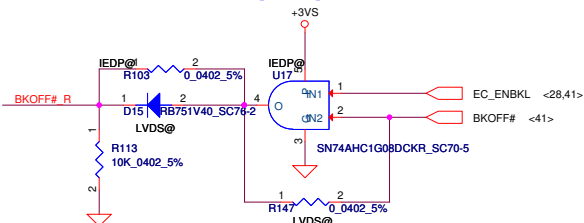
pin11-30 For LVDS or EDP panel



For EMI request , cut in on PVT phase.
Place close CONN.

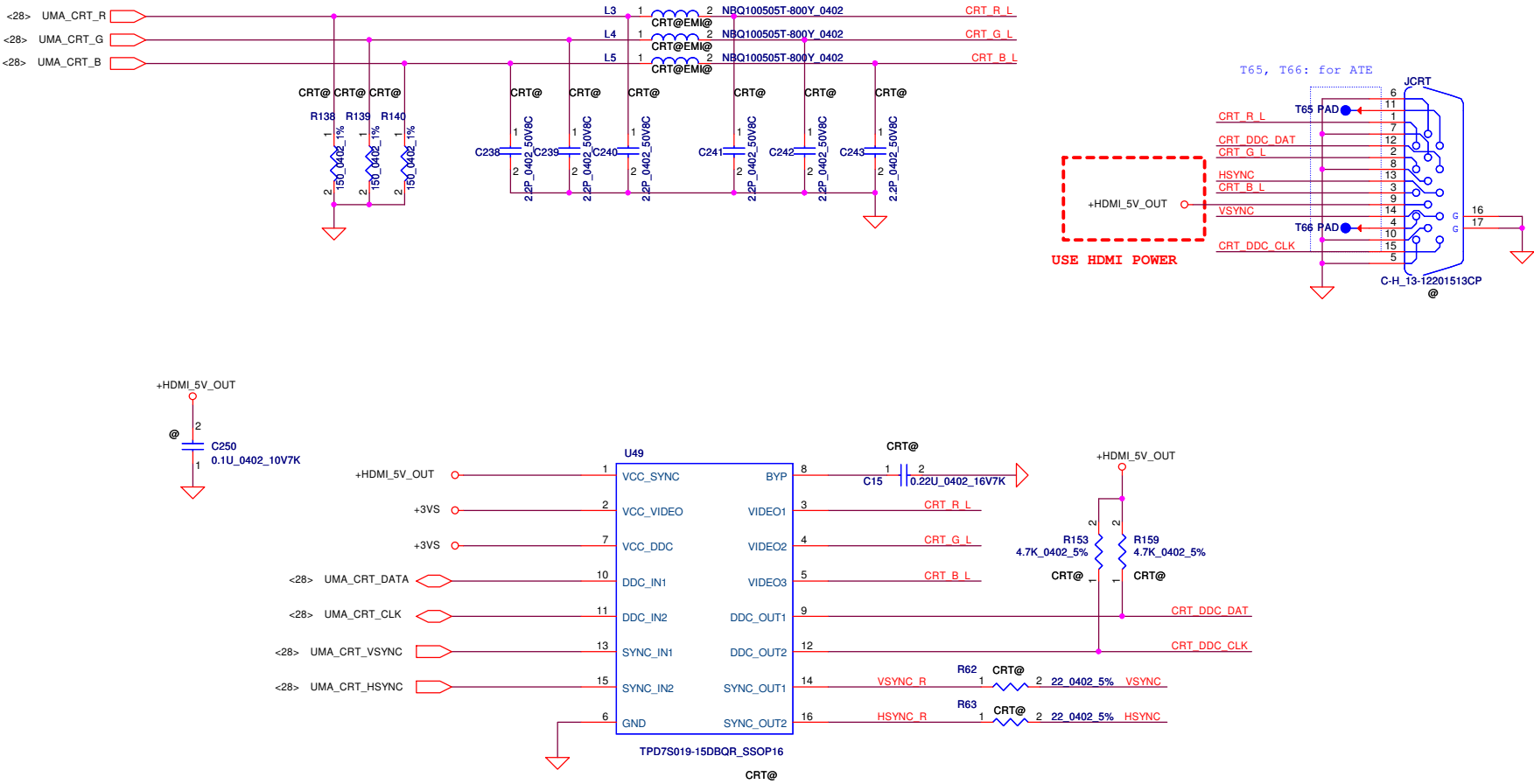


Reserve for eDP panel potential issue

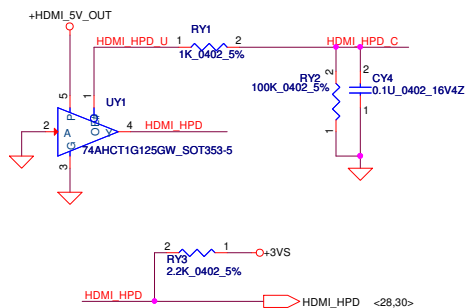
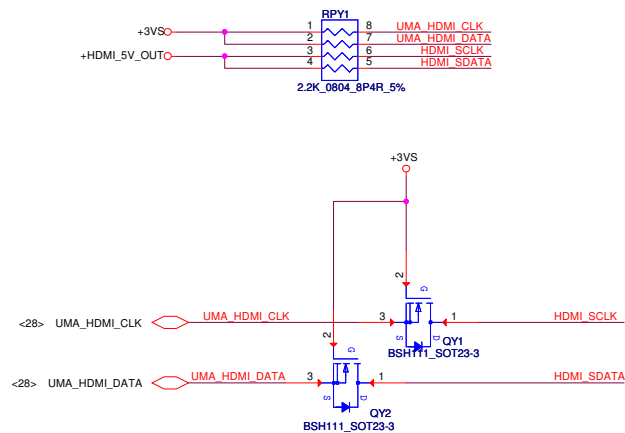


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				VFKTA	
Date:	Thursday, January 17, 2013	Sheet	22	of	56

CRT CONNECTOR

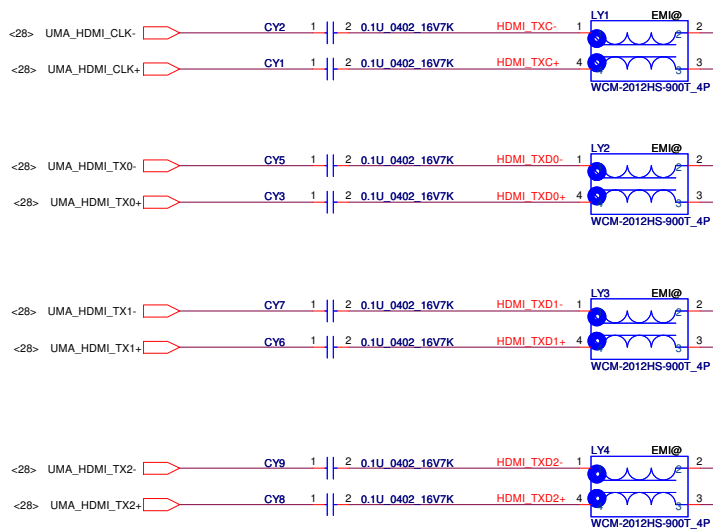
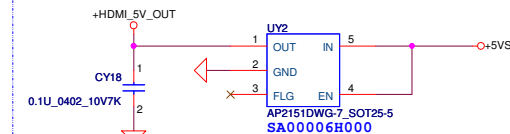


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Issued Date	2012/09/24	Deciphered Date	2013/09/24	Title	
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Size		Document Number			Rev
		VFKTA			0.3
Date:		Thursday, January 17, 2013		Sheet	23 of 56

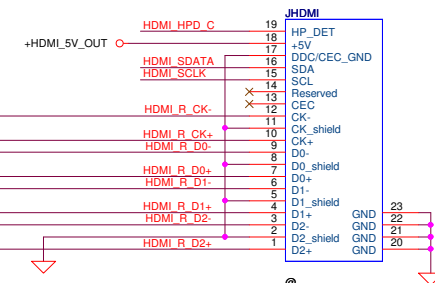


HDMI POWER CIRCUIT

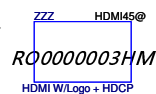
VIN = 5V, IOUT = 0.5A, RDS(ON) TYP=95m ; MAX=115m
Current Limit: TYP=0.8A ; MAX=1A



HDMI Connector



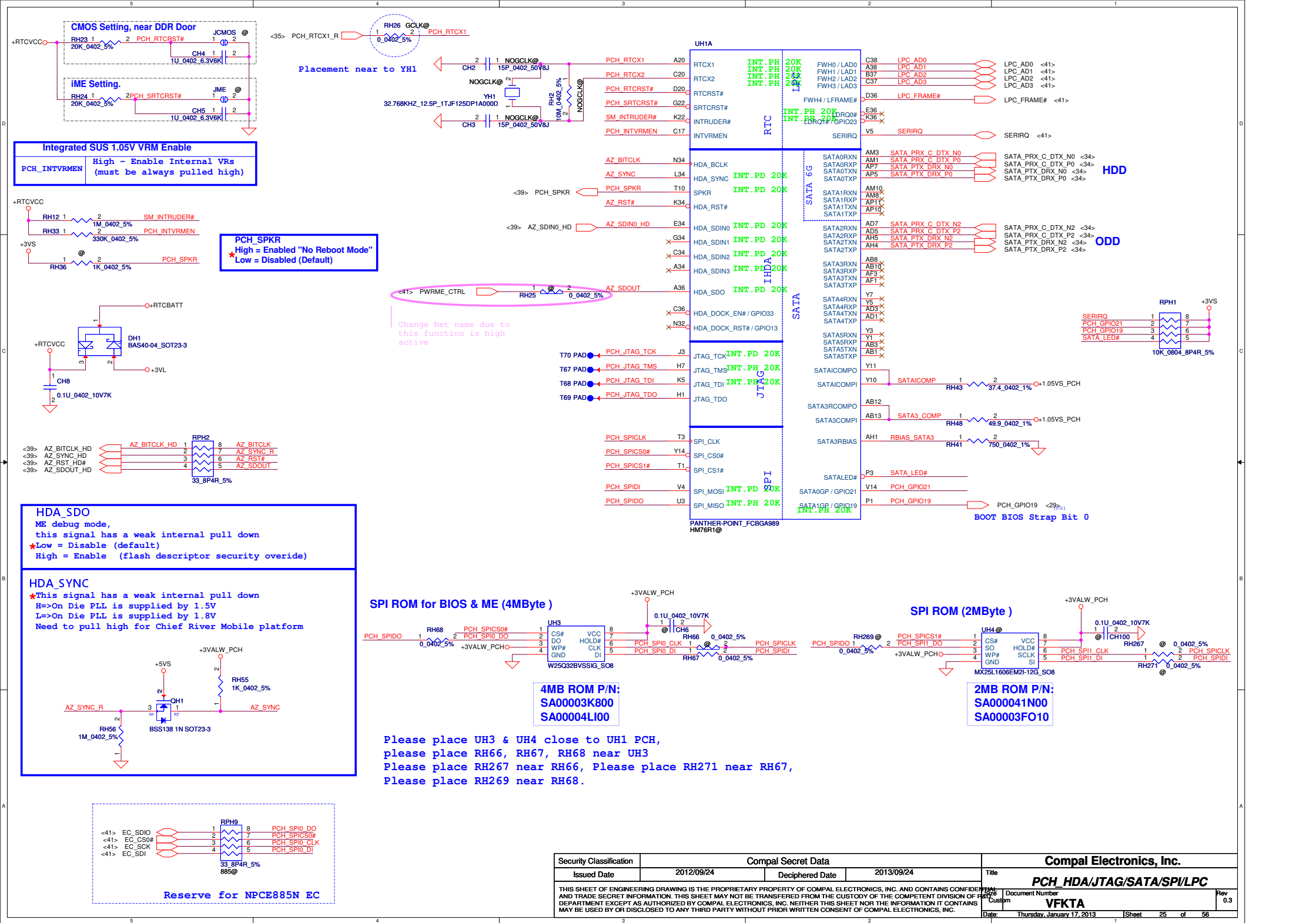
HDMI Royalty

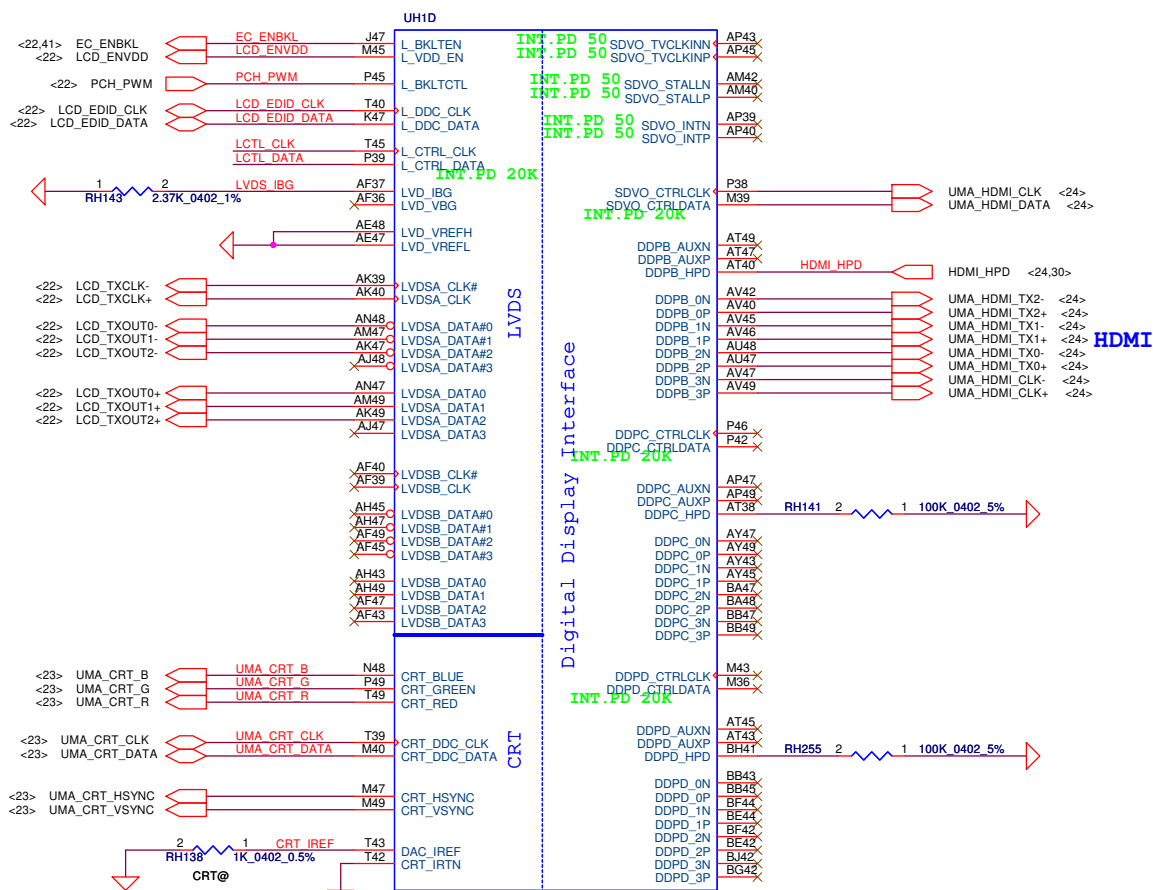
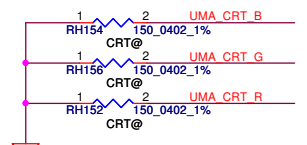
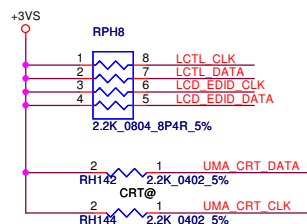
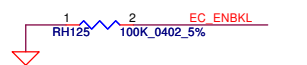


HDMI W/O Logo: RO0000001HM
HDMI W/Logo: RO0000002HM
HDMI W/Logo + HDCP: RO0000003HM

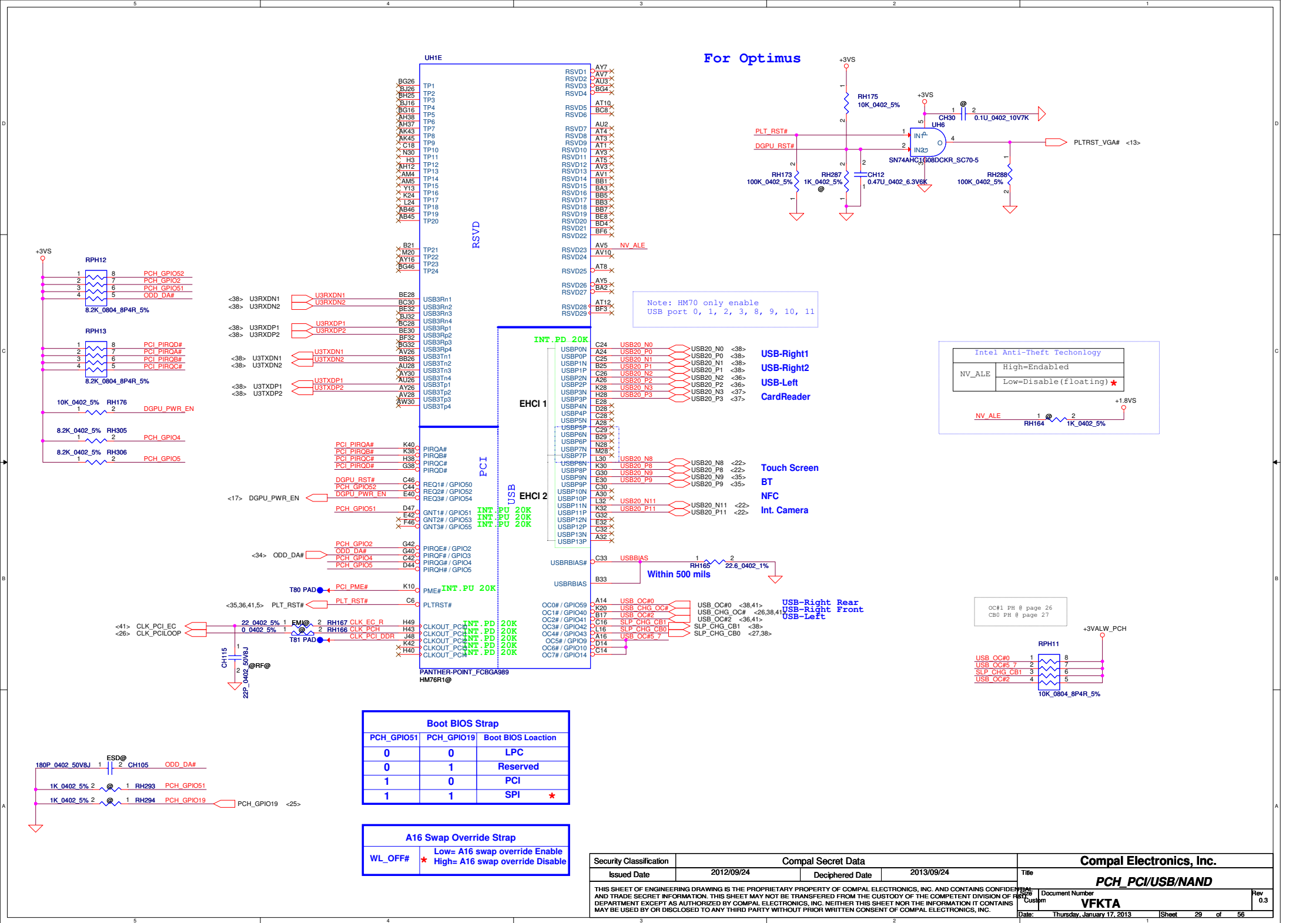
please manually load
this virtual material to 45@ BOM

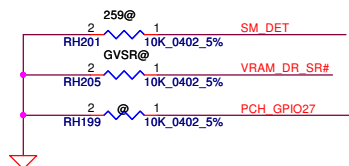
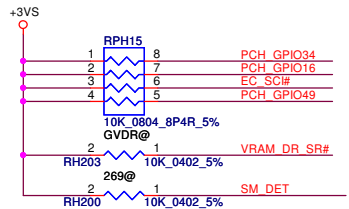
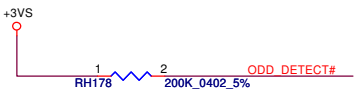
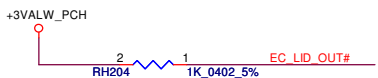
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				Date	Thursday, January 17, 2013	Sheet	24	of	56





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										PCH CRT/LVDS/HDMI	
										VFKTA	
										Date: Thursday, January 17, 2013	
										Sheet 28 of 56	





GPIO28
 On-Die PLL Voltage Regulator
 H: Enable
 L: Disable

GPIO8
 Integrated Clock Chip Enable (Removed)
 H: Disable
 L: Enable

Integrated clock enable functionality is achieved by soft-strap
 The current default is clock enable

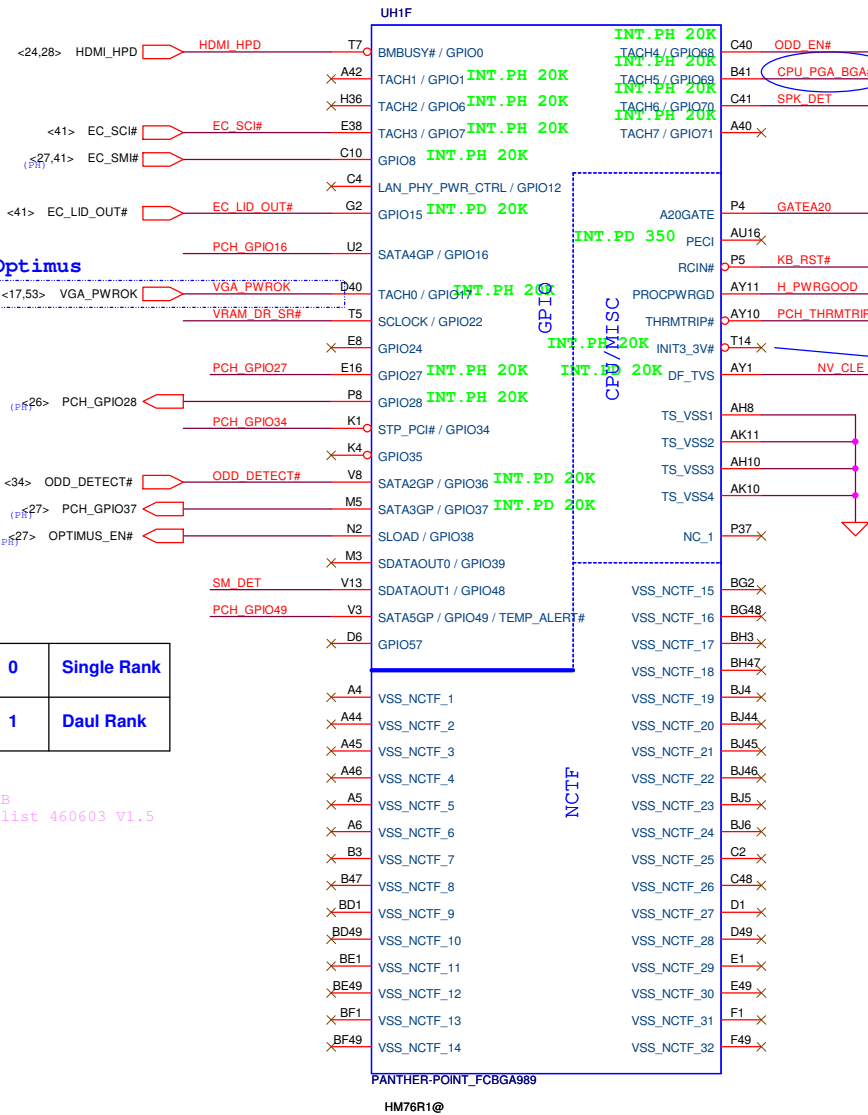
For Optimus

VRAM_DR_SR#	0	Single Rank
	1	Daul Rank

Follow Compal ORB and Intel Check list 460603 V1.5

OPTIMUS_EN#

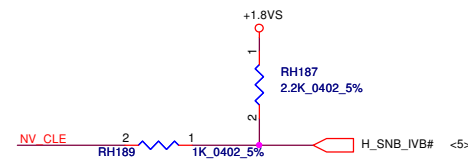
OPTIMUS_EN#	H	L
SKU	NonOPT	Optimus



SM_DET	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	269@
0		Non Harman	259@

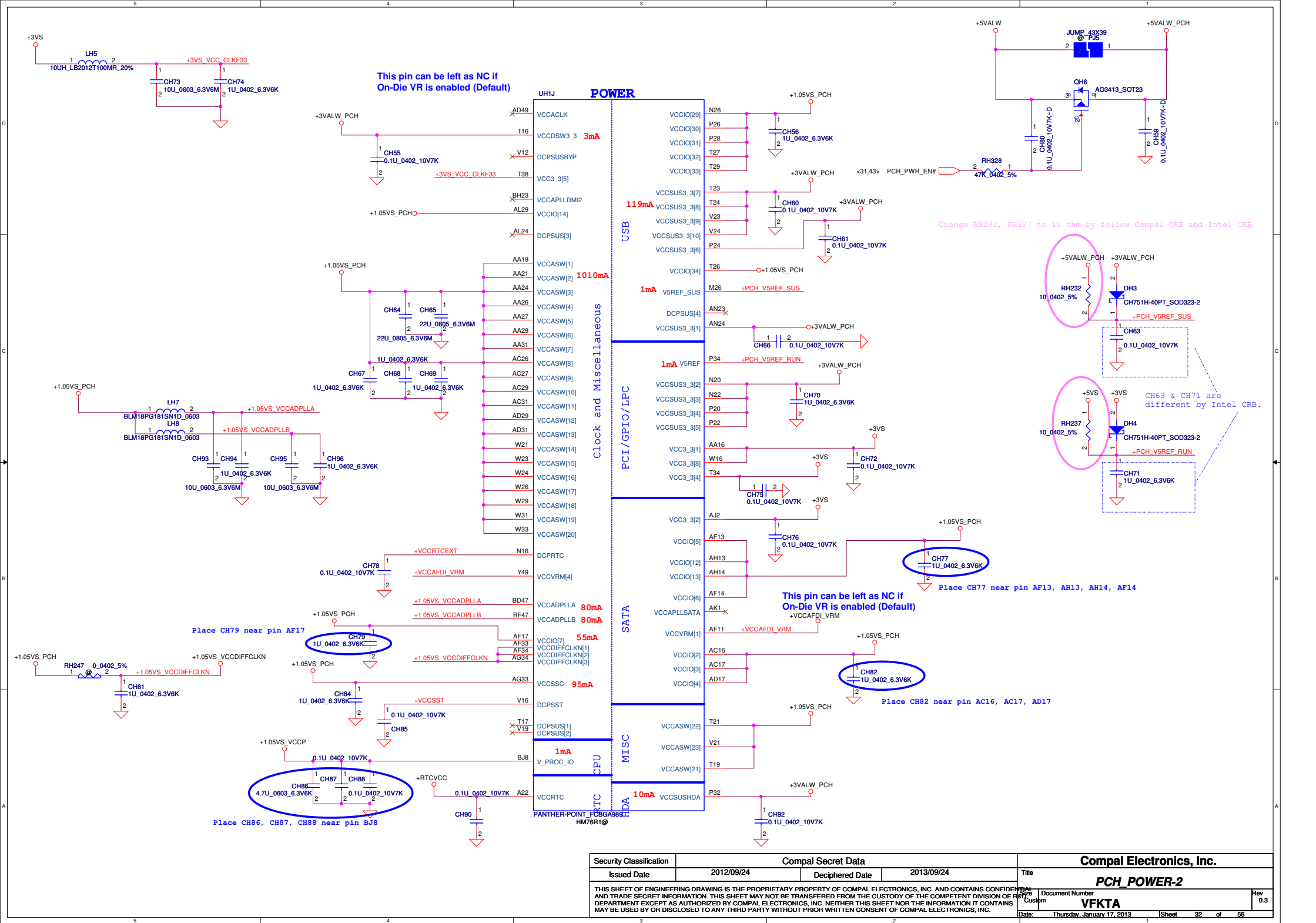
Non-Harman detection		
SPK_DET	0	ONKYO
	1	Non-Brand

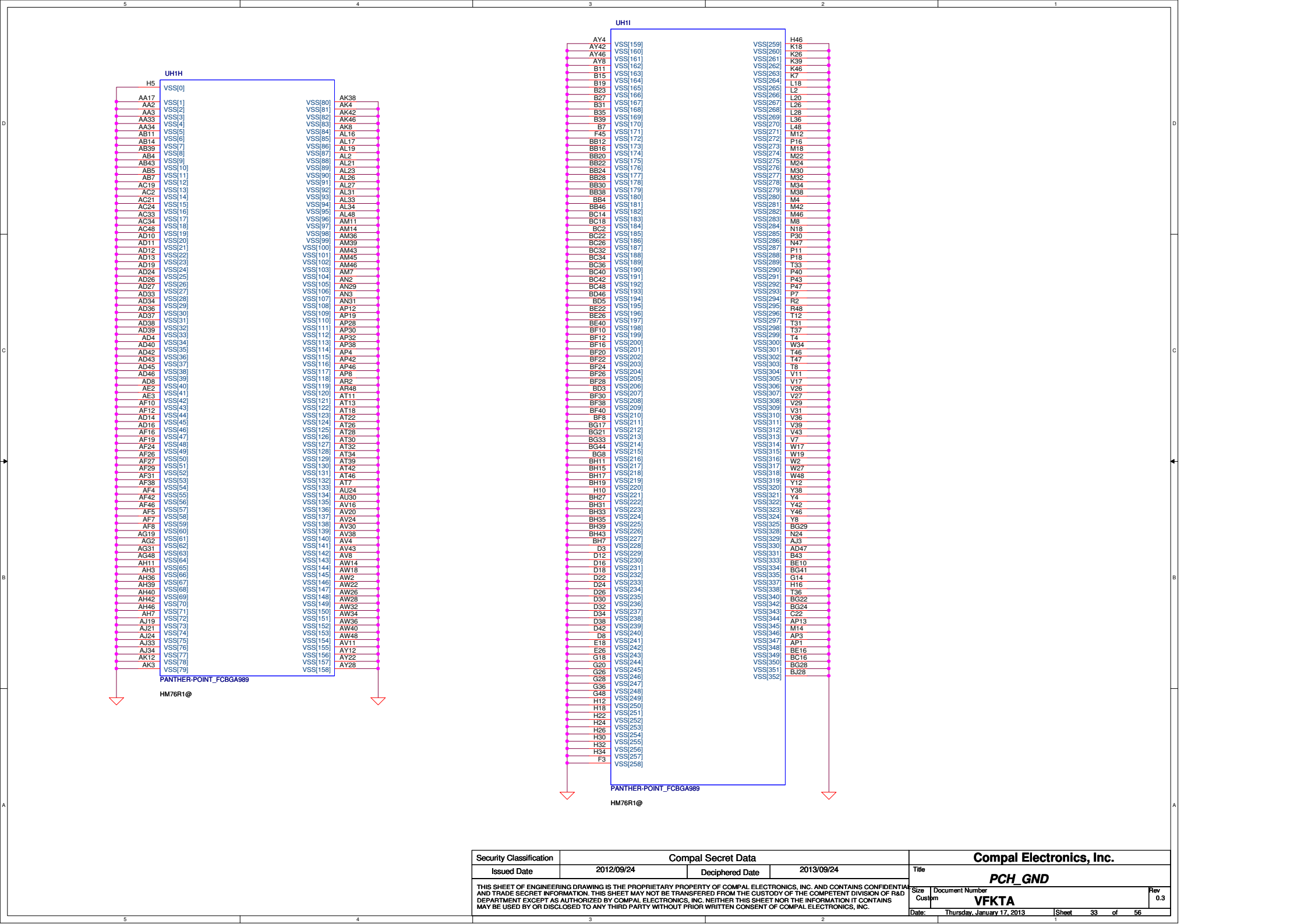
DMI & FDI Termination Voltage	
NV_CLE	Set to VCC when HIGH Set to VSS when LOW



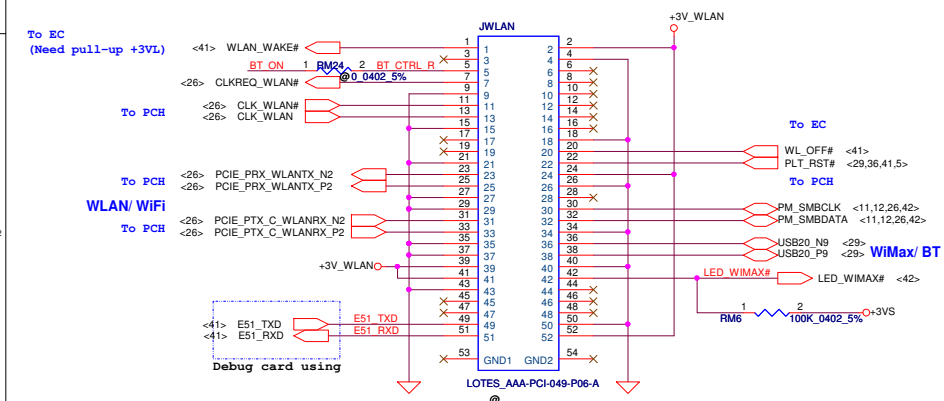
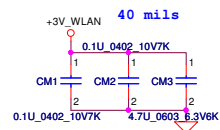
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Size B		Document Number		VFKTA		Rev		0.3			
Date:		Thursday, January 17, 2013		Sheet		30		of 56			

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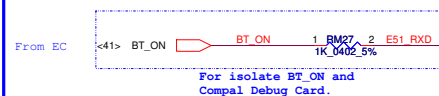


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				VFKTA	
				Date:	Thursday, January 17, 2013
				Sheet	33 of 56
				Rev	0.3

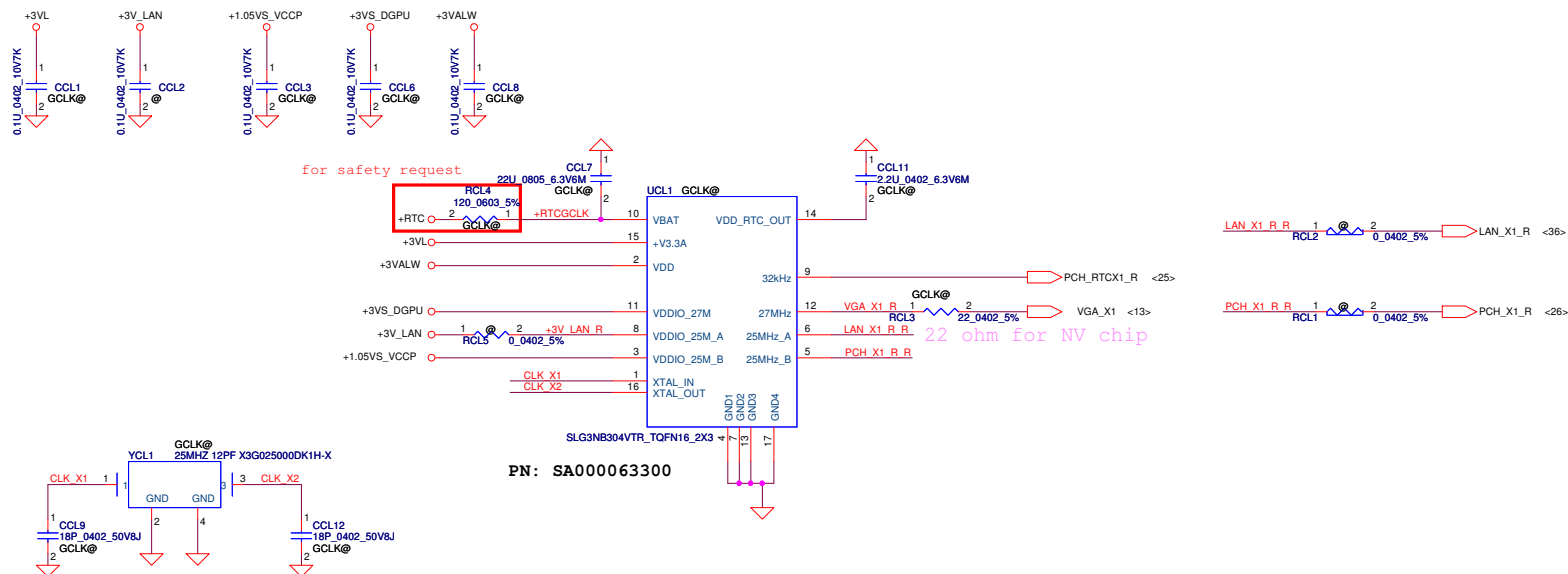
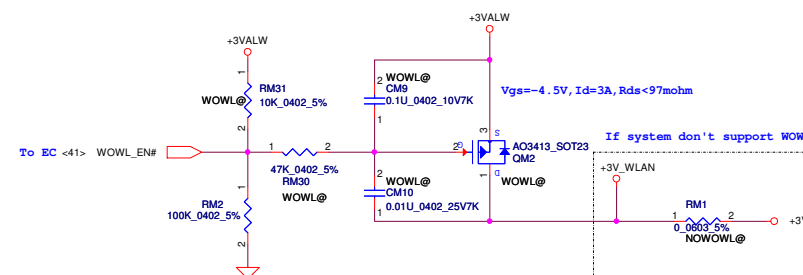
Slot 1 Half PCIe Mini Card-WLAN

WLAN&BT Combo module circuits

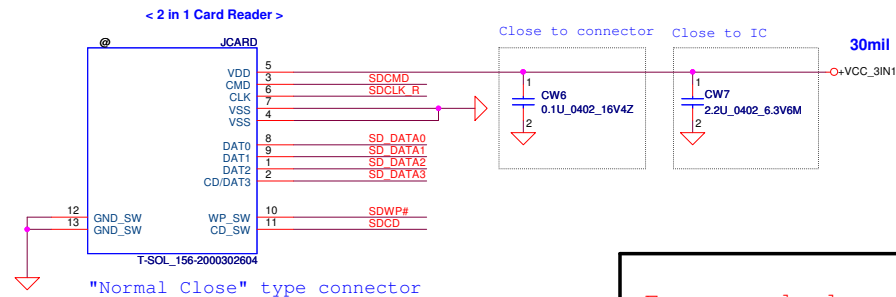
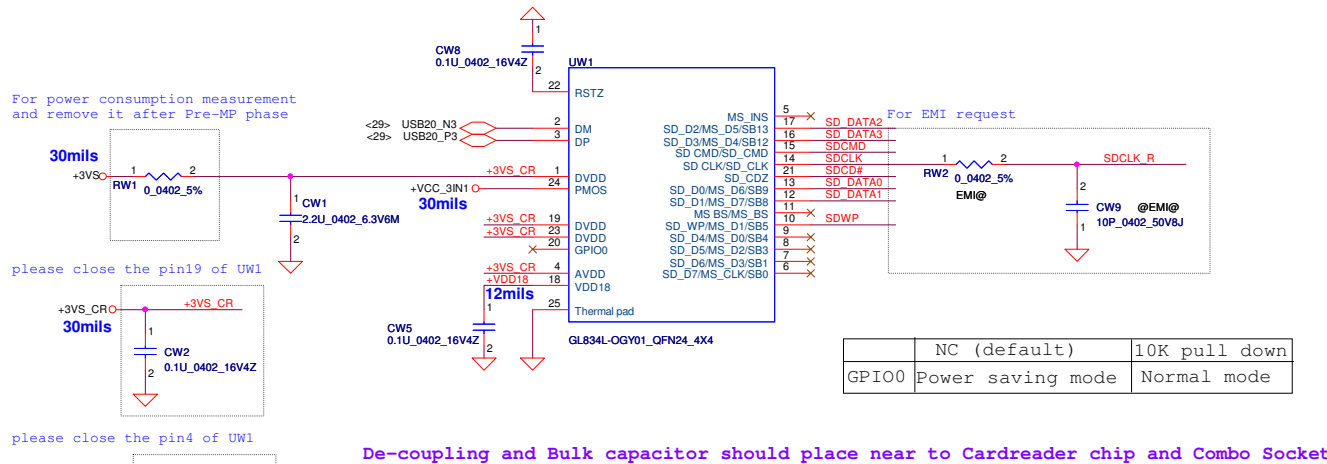
	BT on module Enable	BT on module Disable
BT_ON	H	L



+3VALW TO +3V_WLAN for WOWL

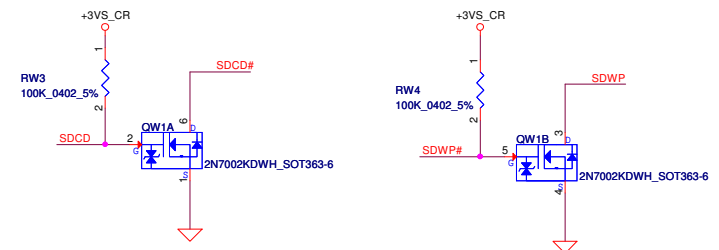


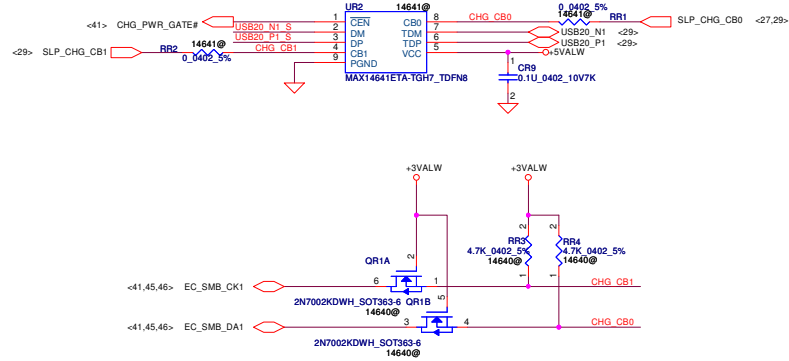
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				VFKTA		
				Date:	Thursday, January 17, 2013	Sheet



	CD_SW	WP_SW	
Card Uninsertion	Close	Protect disable	Protect Enable
		Close	Close
Card Insertion	Open	Open	Close

For normal close type connector invert circuit

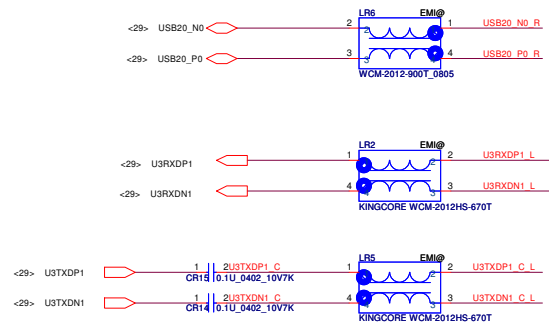




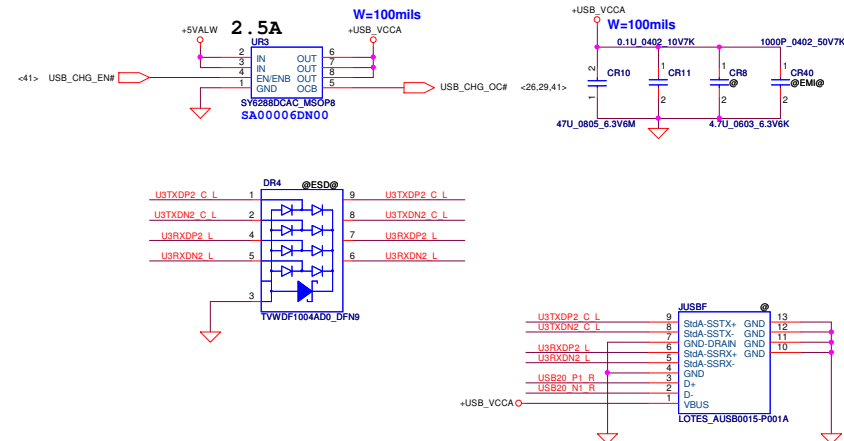
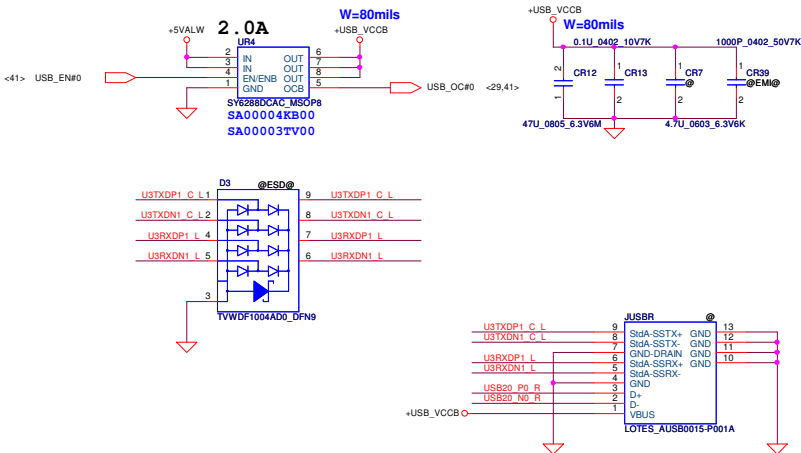
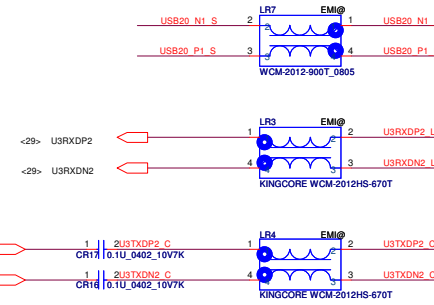
USB Sleep & Charge

State table for MAX14641			
CB0	CB1	Mode	STATUS
0	0	AM2	2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM. Including DCP
0	1	AP1	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	0	PM	USB pass-through mode. DP/DM are connected to TDP/TDM
1	1	CM	USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status.

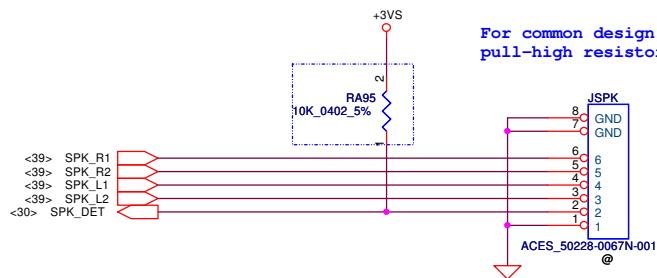
Right rear USB3.0 Conn.



**Right front USB3.0 Conn.
(Support S&C function)**



SPK Conn.



<SM_DET>
Intel : GPIO48
AMD Richland : GPIO173
AMD Kabini : GPIO70

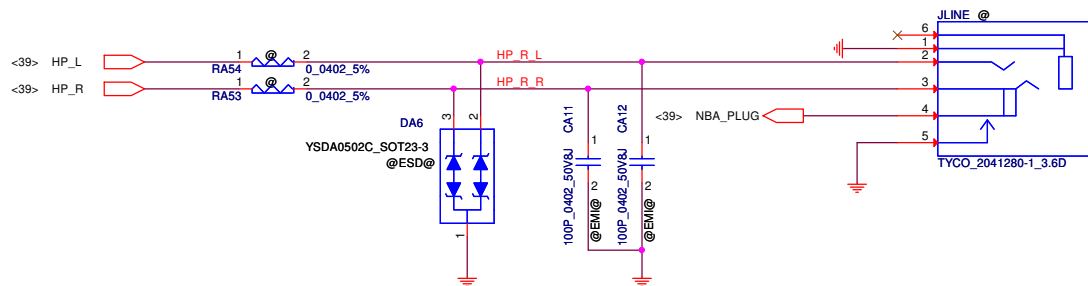
<SPK_DET>
Intel : GPIO70
AMD Richland : GPIO74
AMD Kabini : GPIO62

SM_DET	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	269@
0		Non Harman	259@

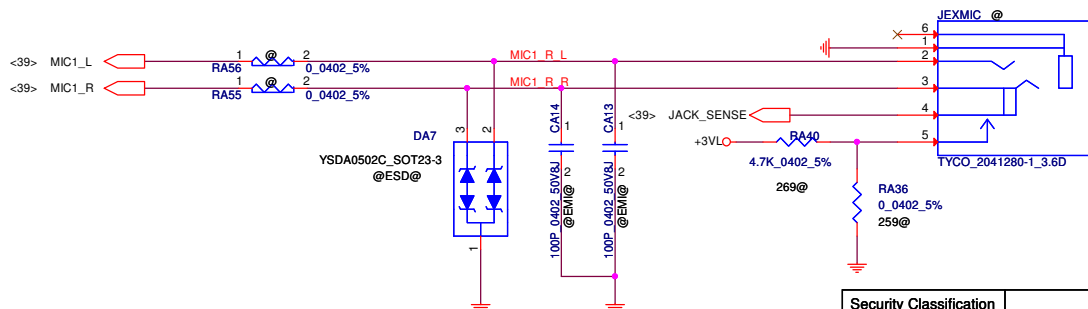
Non-Harman detection

SPK_DET	0	ONKYO
SPK_DET	1	Non-Brand

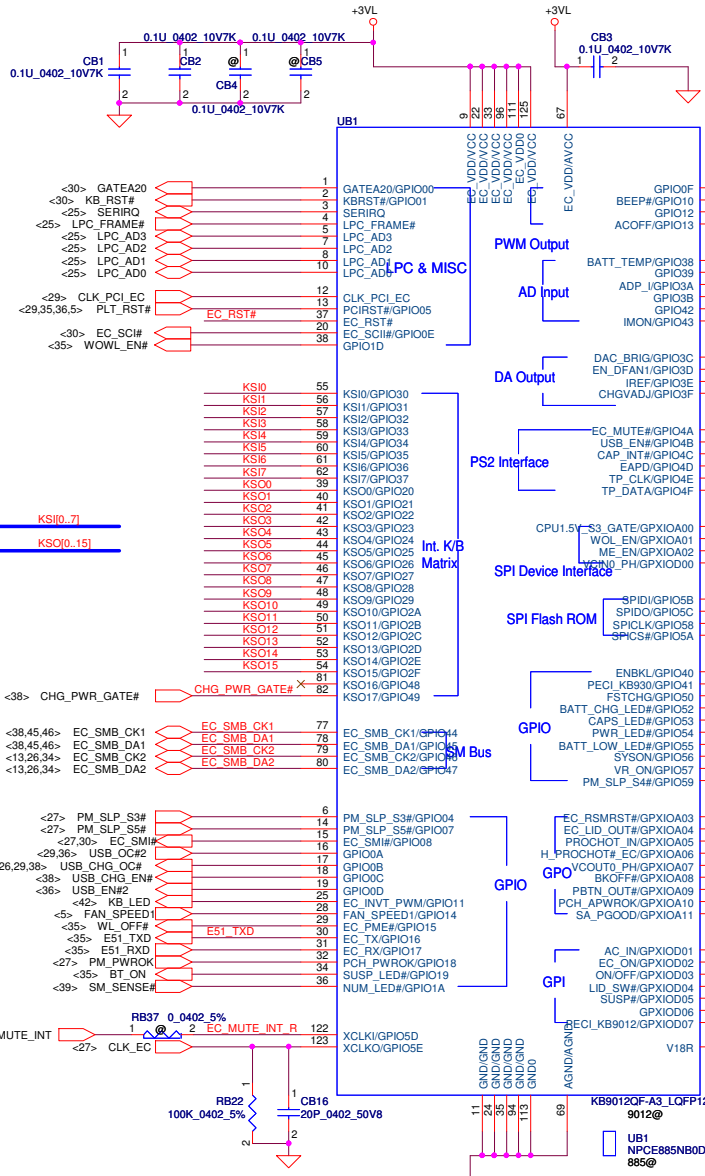
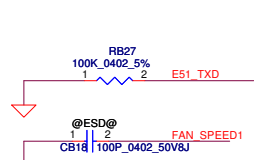
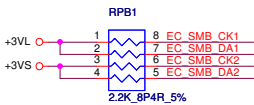
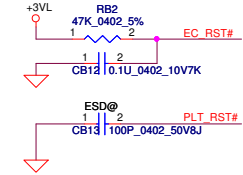
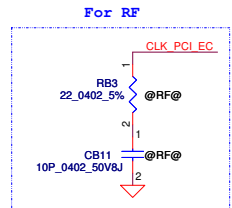
HeadPhone/LINE Out JACK



MIC/LINE IN JACK

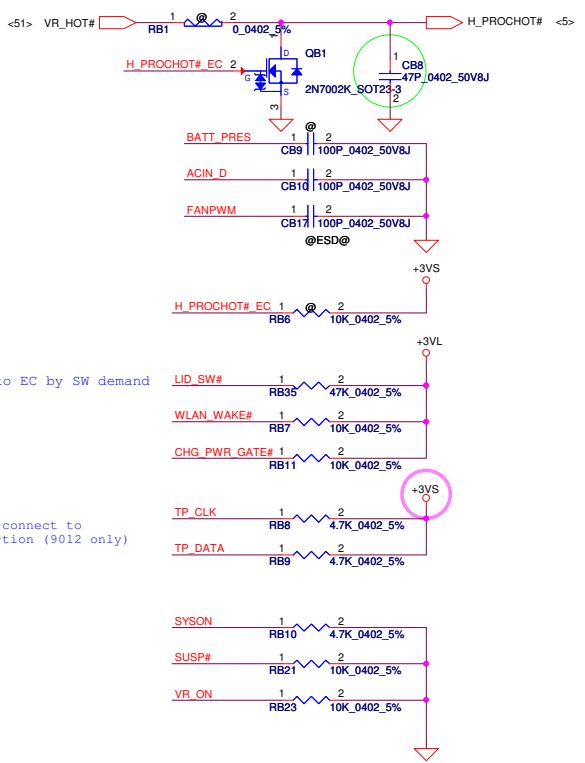
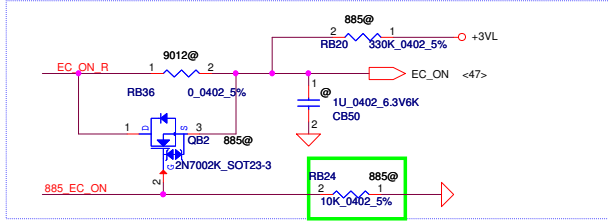


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Date:	Thursday, January 17, 2013	Sheet	40	of 56

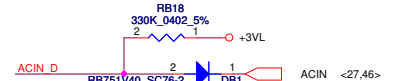


Voltage Comparator Pins FOR 9012 A3

VCIN0 pin109	>1.2V	<1.2V
VCOUT0 pin104	HIGH (default)	LOW
VCOUT1 pin103	HIGH	LOW (default)



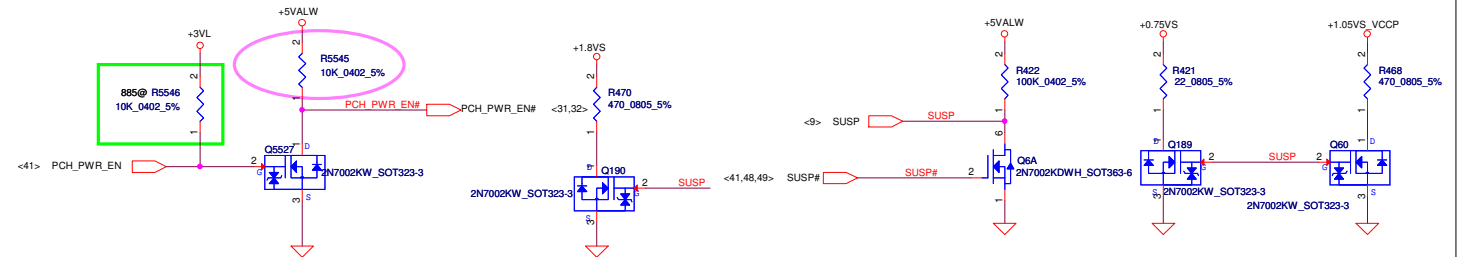
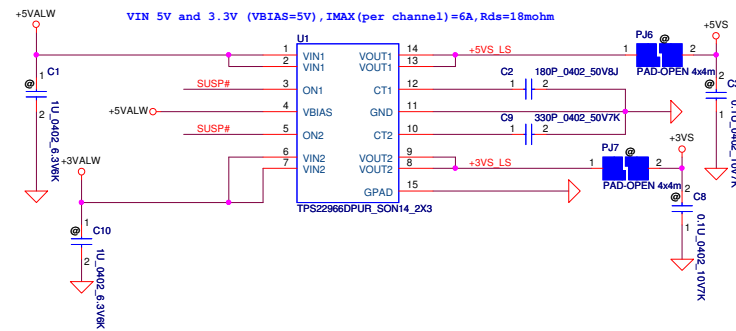
VCOUT0_PH_L 1 2 0.0402_5% VS_ON <47>
VCOUT0_PH connect to power portion (9012 only)



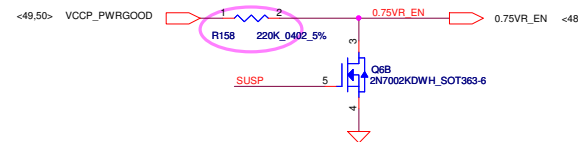
Close to EC



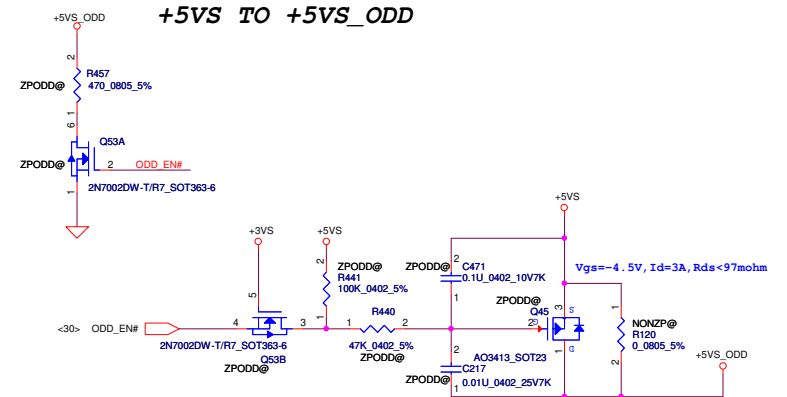
+5VALW TO +5VS
+3VALW TO +3VS
Load switch



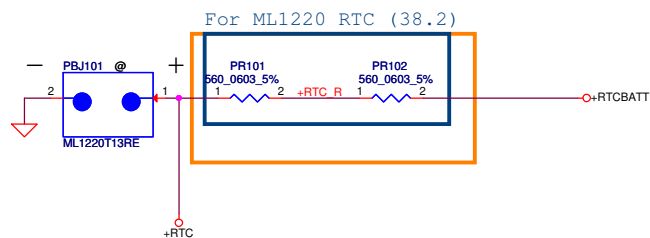
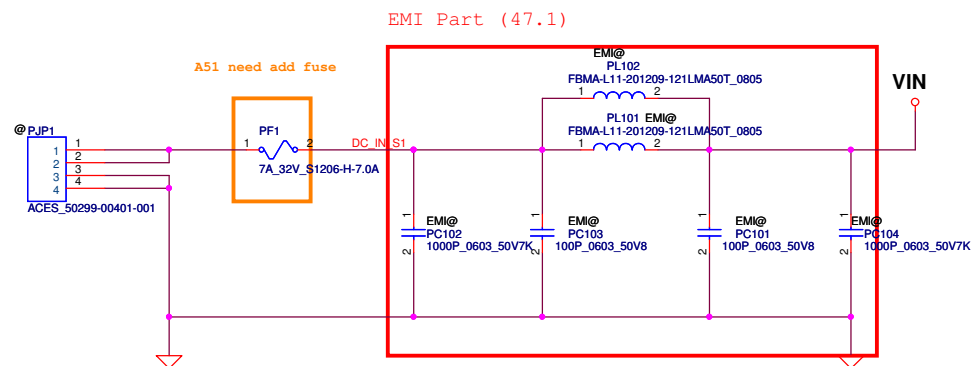
For S3 CPU Power Saving



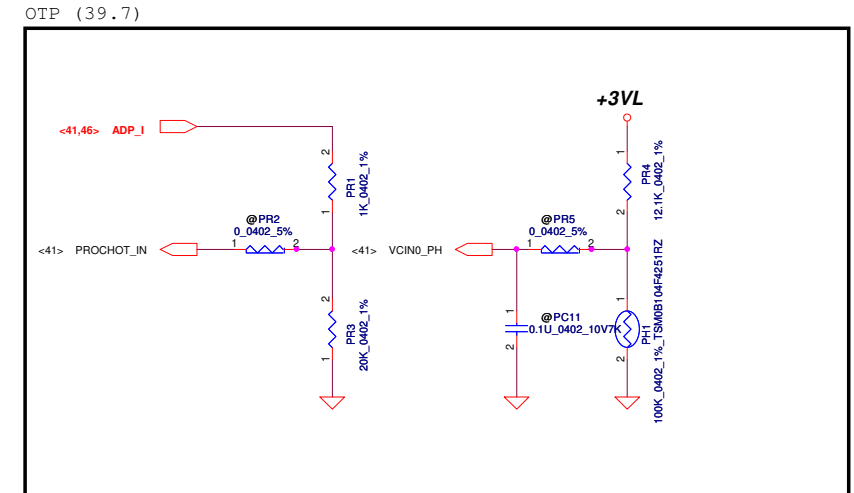
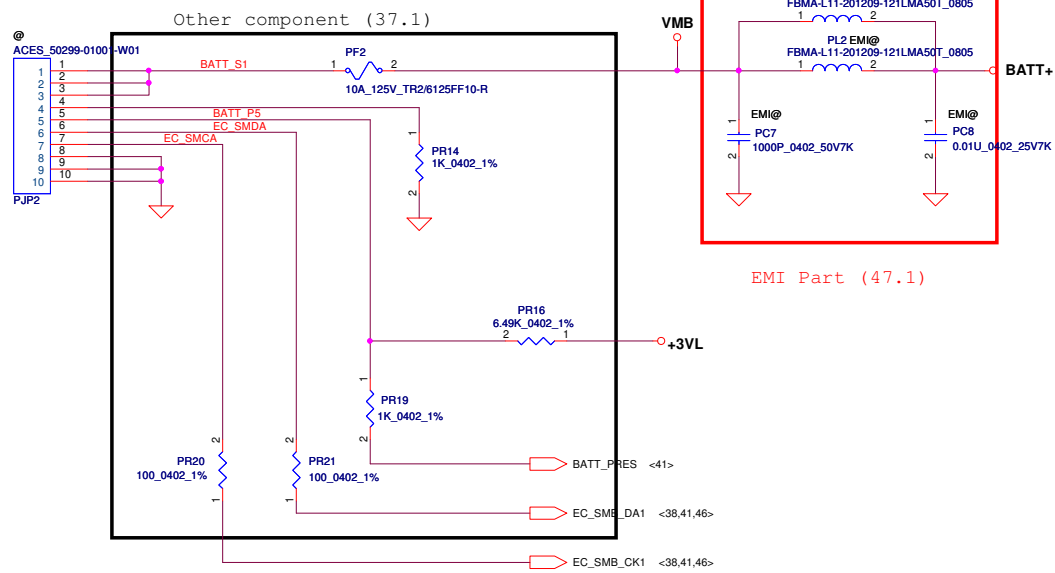
+5VS TO +5VS_ODD



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				Date	Thursday, January 17, 2013
				Sheet	43 of 56
				Rev	0.3

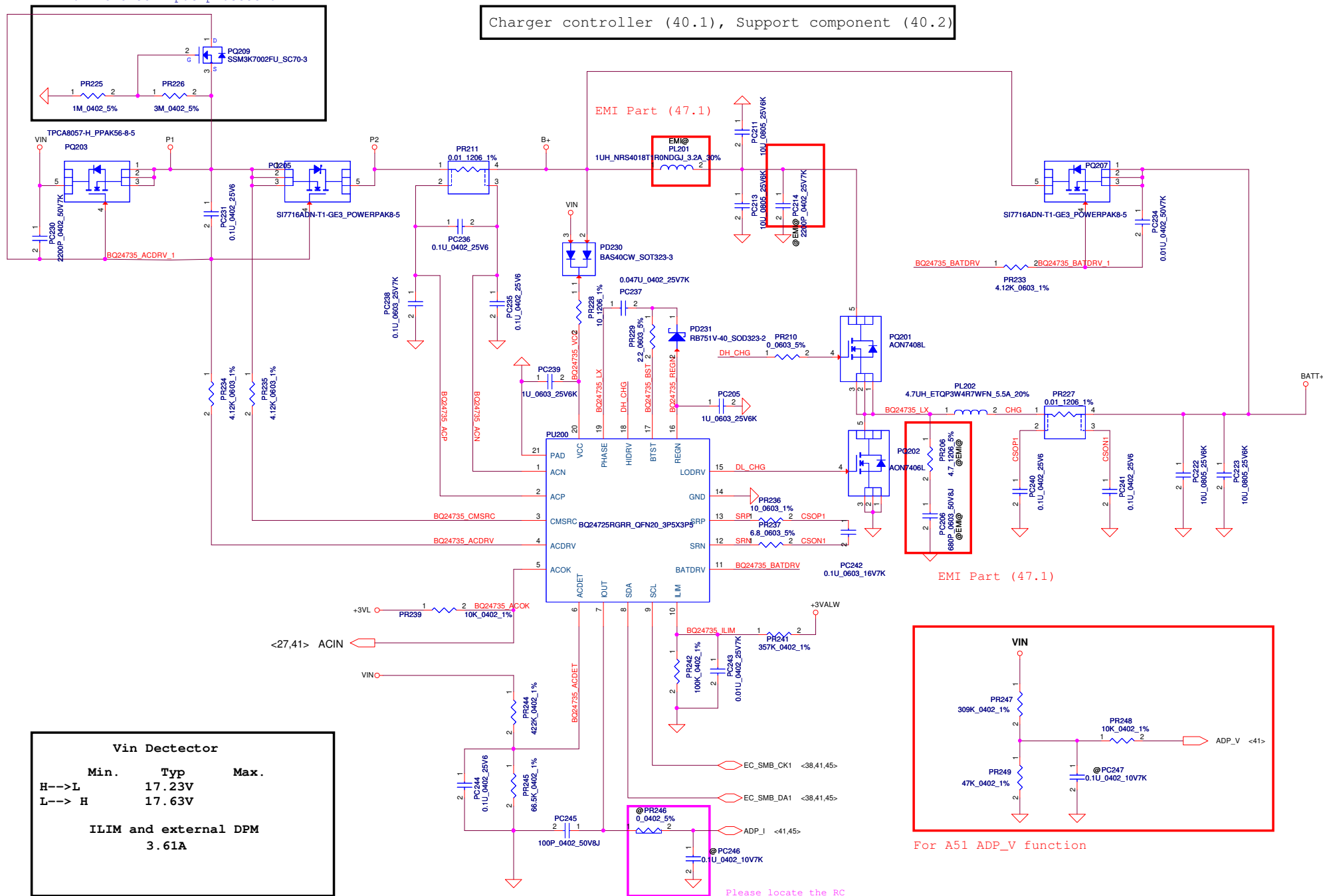


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/09/24	Deciphered Date	2013/09/24	Title	DCIN/PRECHARGE
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				Document Number	VFKTA
				Rev	0.3
				Date:	Sheet 44 of 56



for reverse input protection

Charger controller (40.1), Support component (40.2)



Vin Detector

	Min.	Typ	Max.
H-->L		17.23V	
L--> H		17.63V	

ILIM and external DPM
3.61A

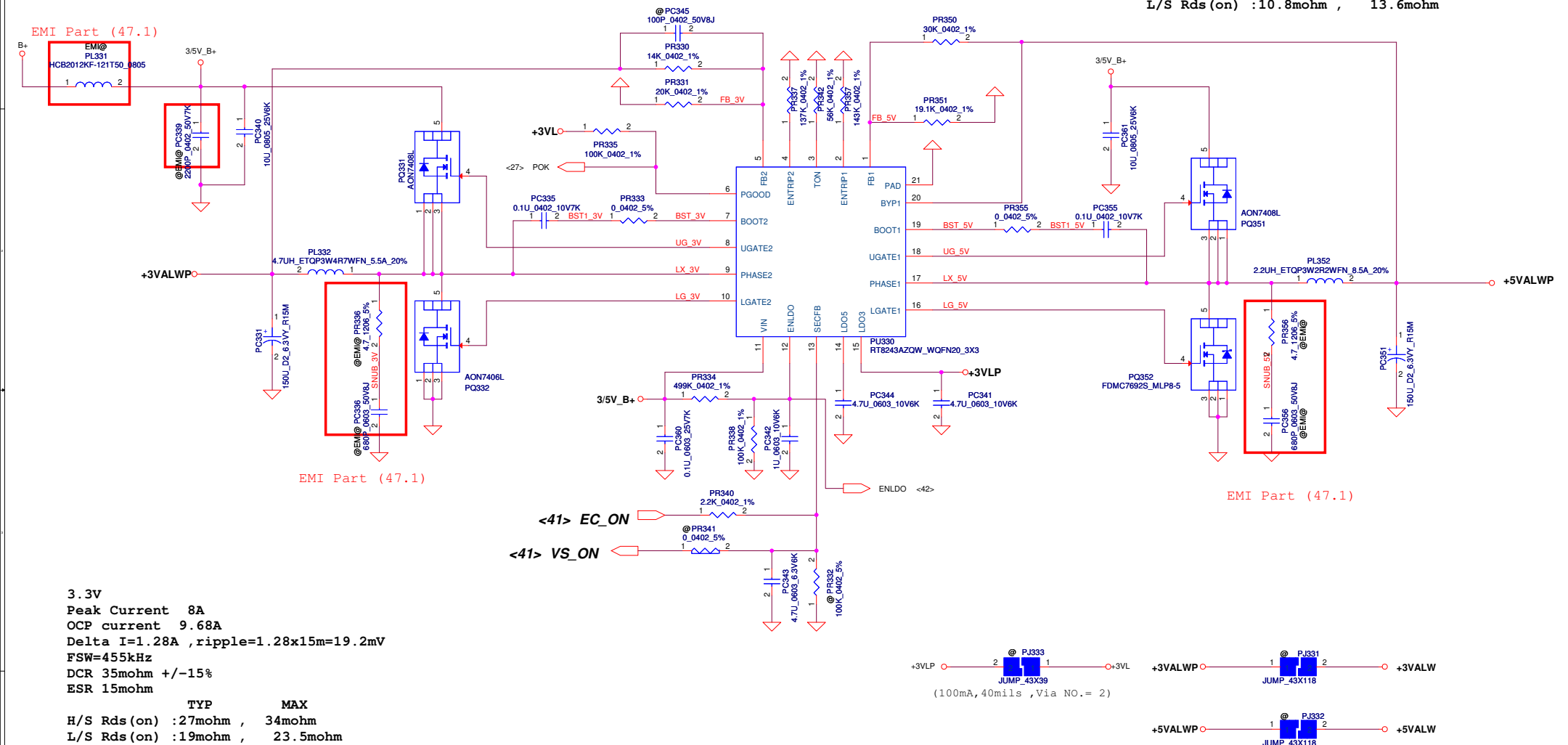
Please locate the RC
Near EC chip
2011-02-22

For A51 ADP_V function

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Issued Date	2012/09/24	Deciphered Date	2013/09/24	Document Number	Size	Customer	Rev
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				Date:		Sheet	46 of 56

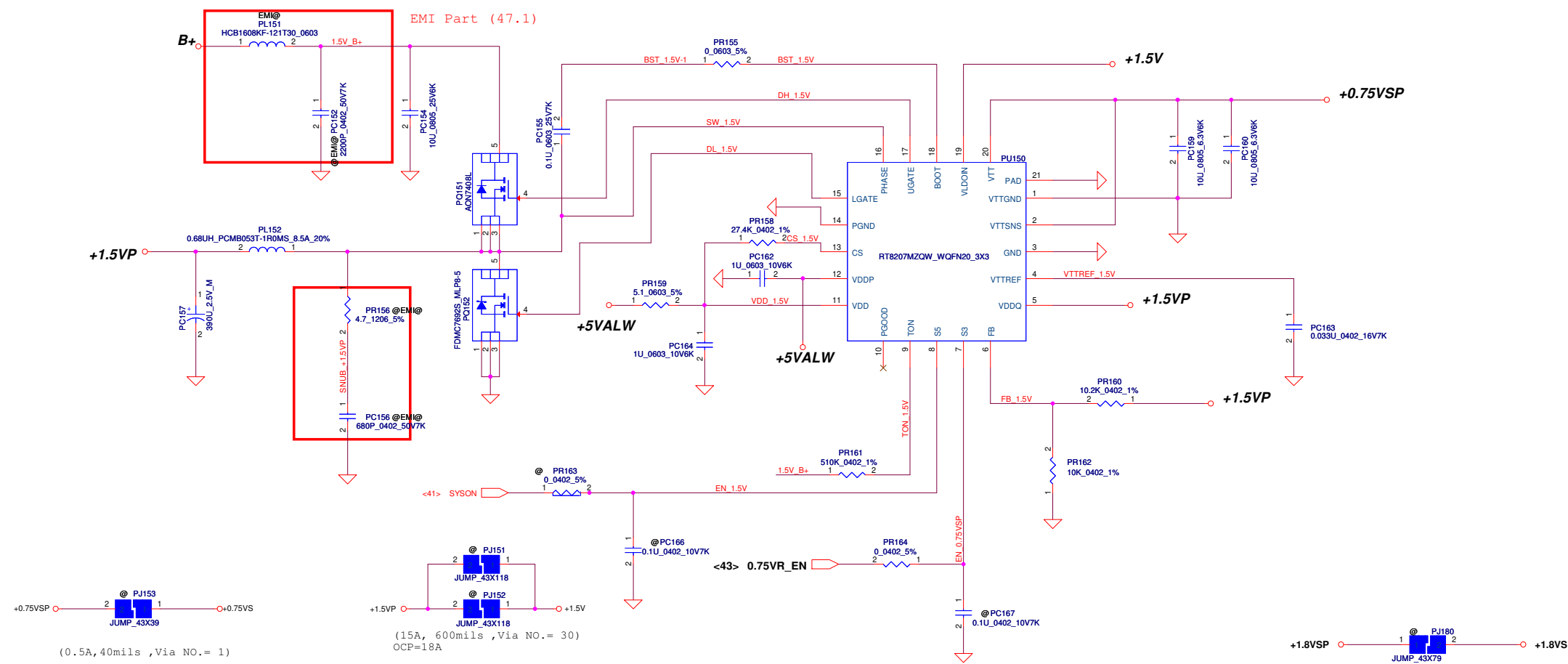
5V
Peak Current 10A
OCP current 12.03A
FSW=390kHz
Delta I=4.29A, ripple=4.29*17m=72.93mV
DCR 15.5mohm+/-15%
ESR 17mohm

	TYP	MAX
H/S Rds(on)	:27mohm	34mohm
L/S Rds(on)	:10.8mohm	13.6mohm



Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2012/09/24	Deciphered Date	2013/09/24	Title	3VALW/5VALW		
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				Custom	VFKTA	0.3	
Date:		Sheet	47	of	56		

DDR controller (35.3), Support component (35.4)



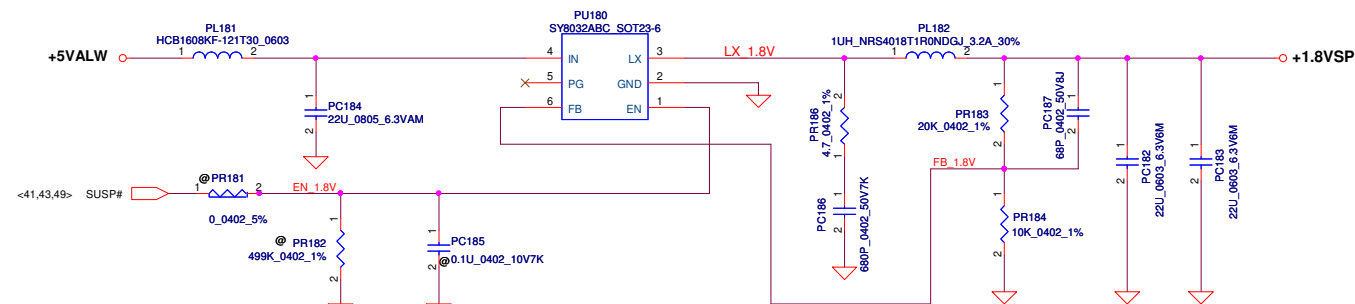
1.5V
Peak Current 16.8A
OCF current 20 A
FSW=495kHz
DCR 13mohm
ESR 9mohm

	TYP	MAX
H/S Rds (on)	:27mohm	34mohm
L/S Rds (on)	:10.8mohm	13.6mohm

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

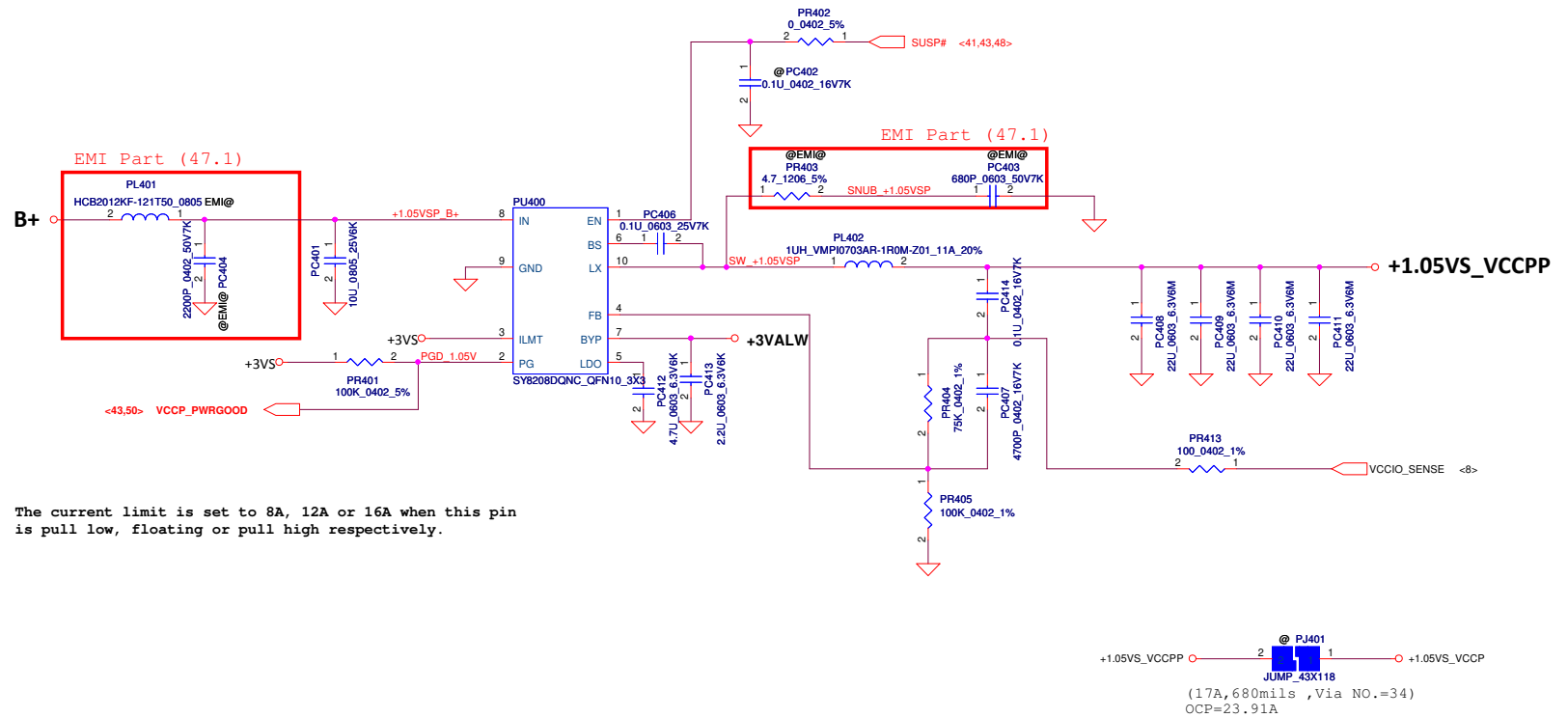
Note: S3 - sleep ; S5 - power off

1.8VS controller (35.15), Support component (35.16)



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						Size	Document Number	Rev
						Custom	VFKTA	0.1
						Date:	Sheet	48 of 56

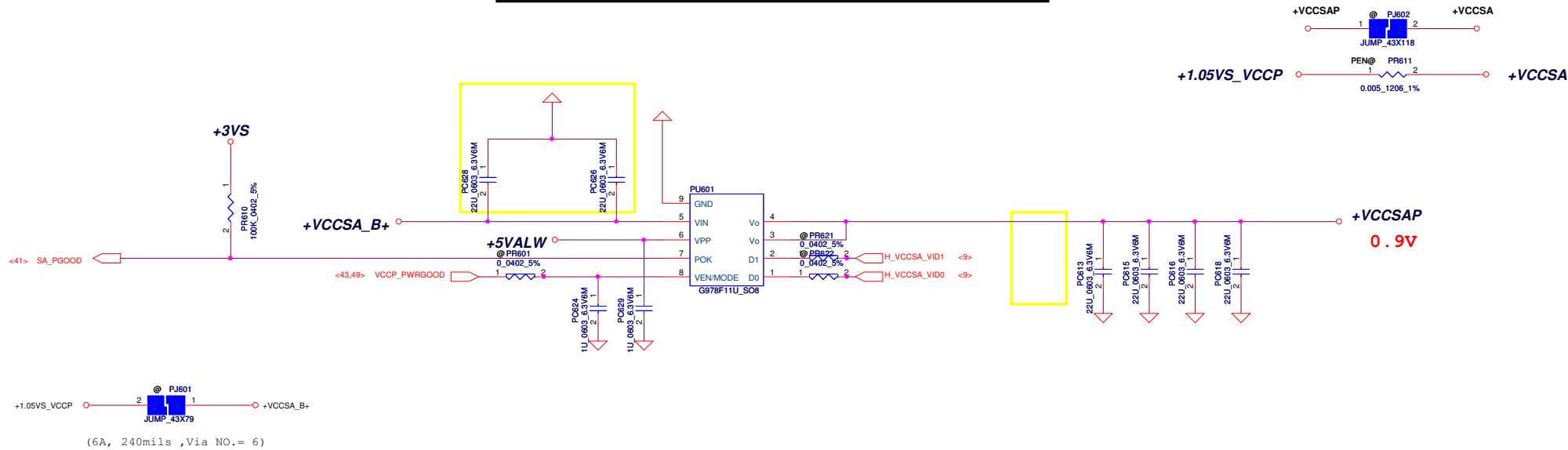
1.05VCCP controller (35.5), Support component (35.6)



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Issued Date		2012/09/24		Deciphered Date		2013/09/24		Title			
								+1.05VS VCCP			
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								VKFTA		0.3	
						Date:		Thursday, January 17, 2013		Sheet	

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

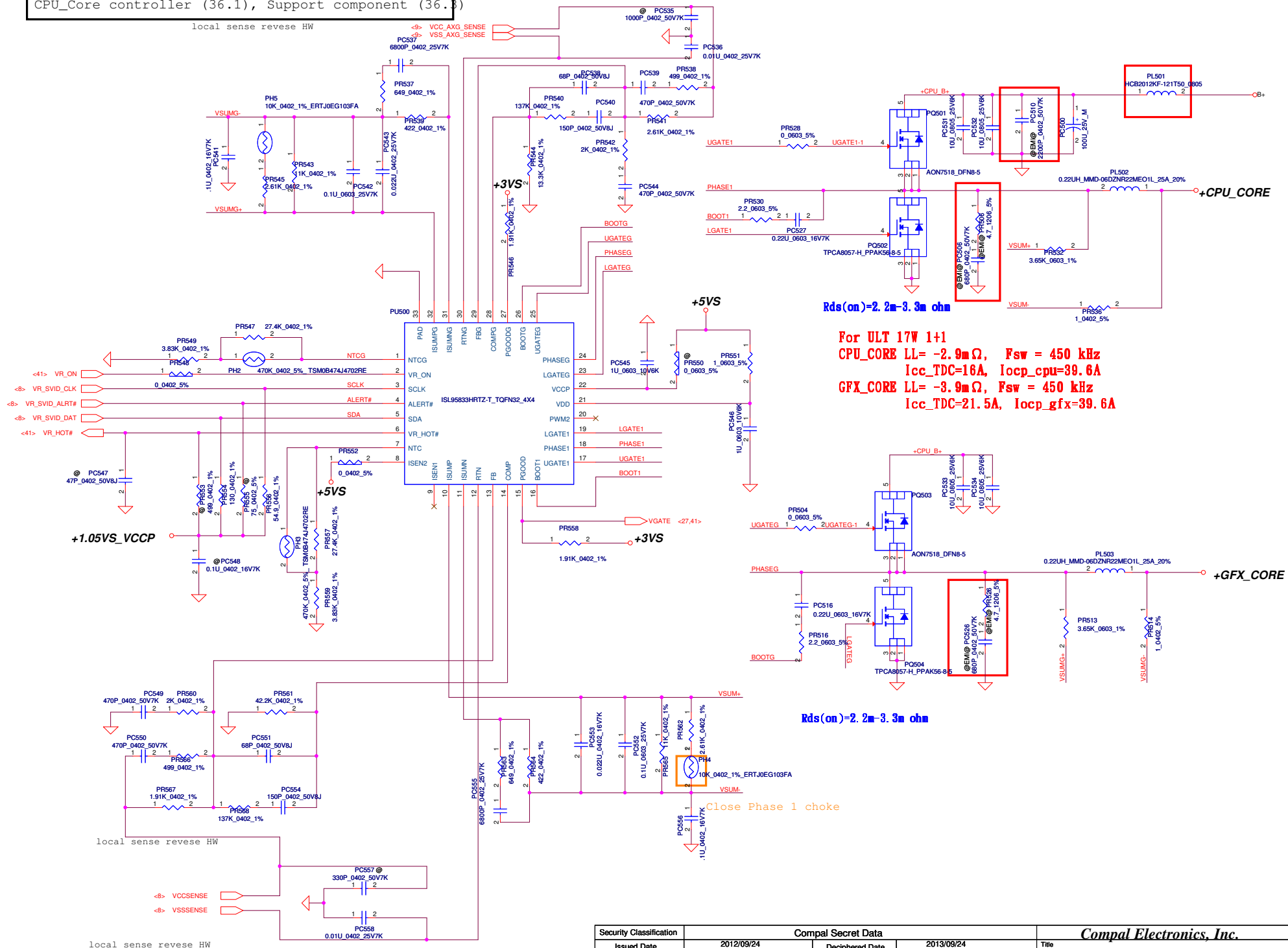
VCCSA controller (35.17), Support component (35.18)



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/09/24	Deciphered Date	2013/09/24	Title	VCC_SAP	
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				Custom	VFKTA	0.3
				Date:	Sheet 50 of 56	

CPU_Core controller (36.1), Support component (36.3)

local sense reverse HW



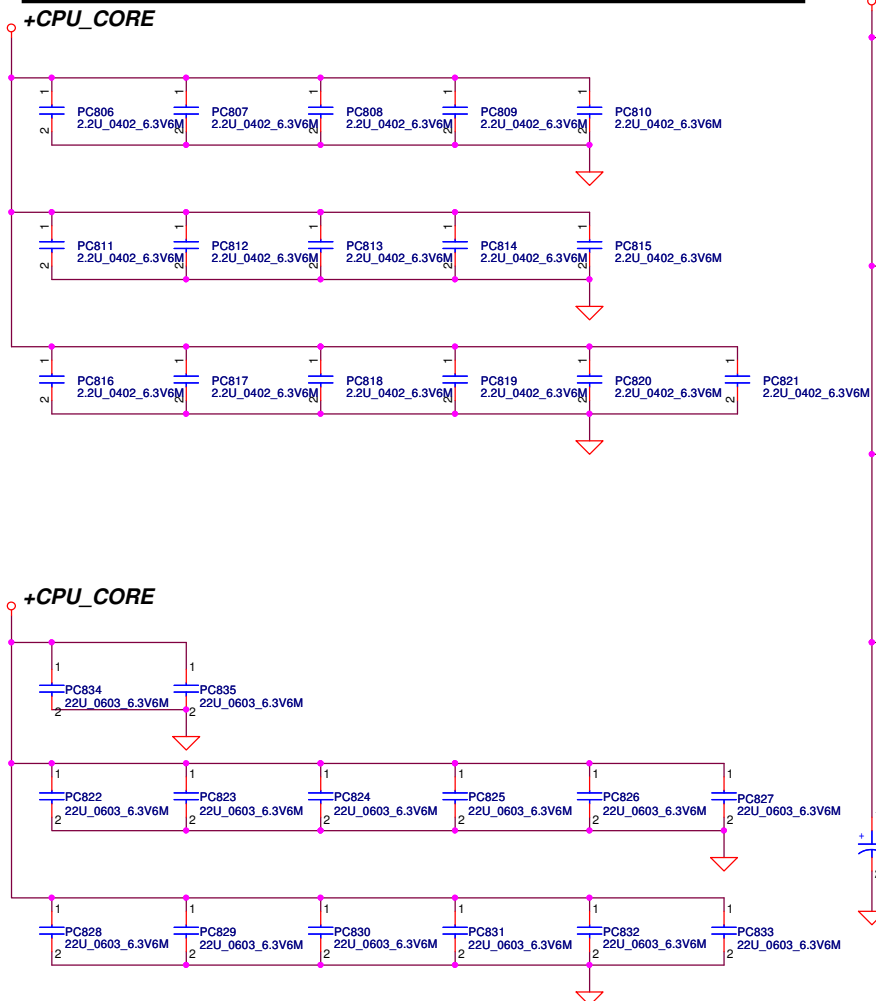
For ULT 17W 1+1
CPU_CORE LL= -2.9mΩ, Fsw = 450 kHz
Icc_TDC=18A, Iocp_cpu=39.6A
GFX_CORE LL= -3.9mΩ, Fsw = 450 kHz
Icc_TDC=21.5A, Iocp_gfx=39.6A

Rds(on)=2.2m-3.3m ohm

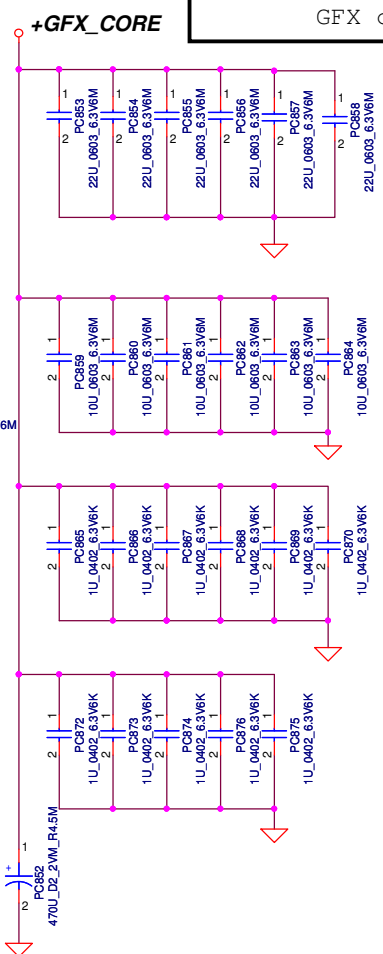
Close Phase 1 choke

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Issued Date	2012/09/24	Deciphered Date	2013/09/24	Title	CPU CORE
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				Date	Thursday, January 17, 2013
				Sheet	51 of 56
				Rev	0.3

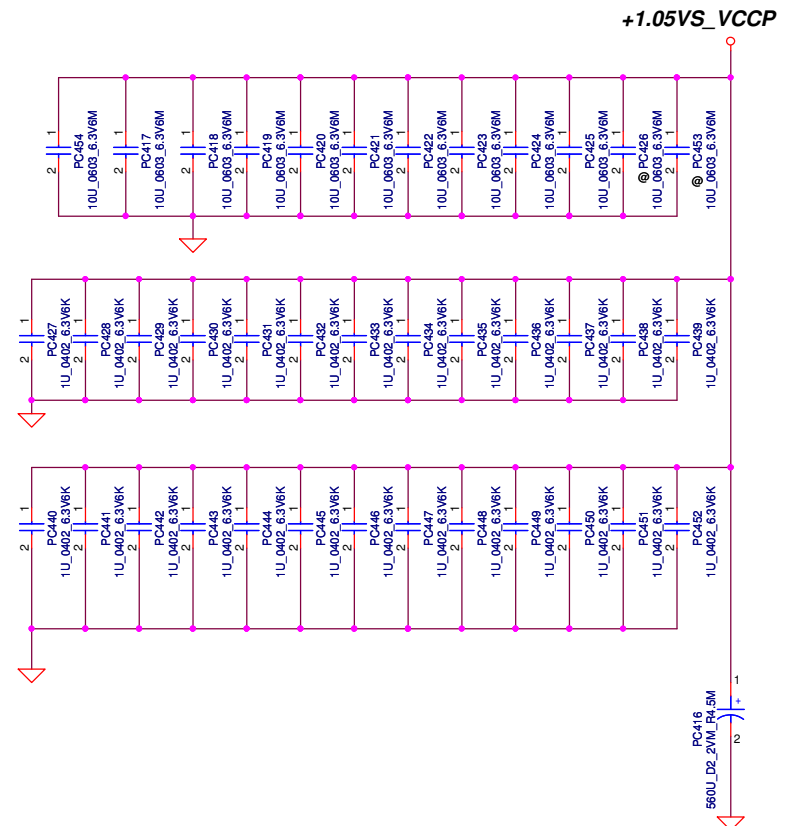
CPU_Core output CAP (Including MLCC) 36.4



GFX output CAP (Including MLCC) 36.5

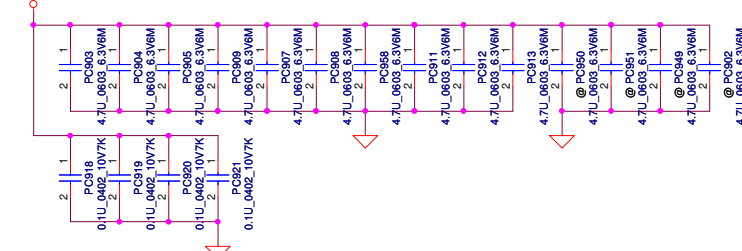


VCCP output Cap (Including MLCC) 36.6

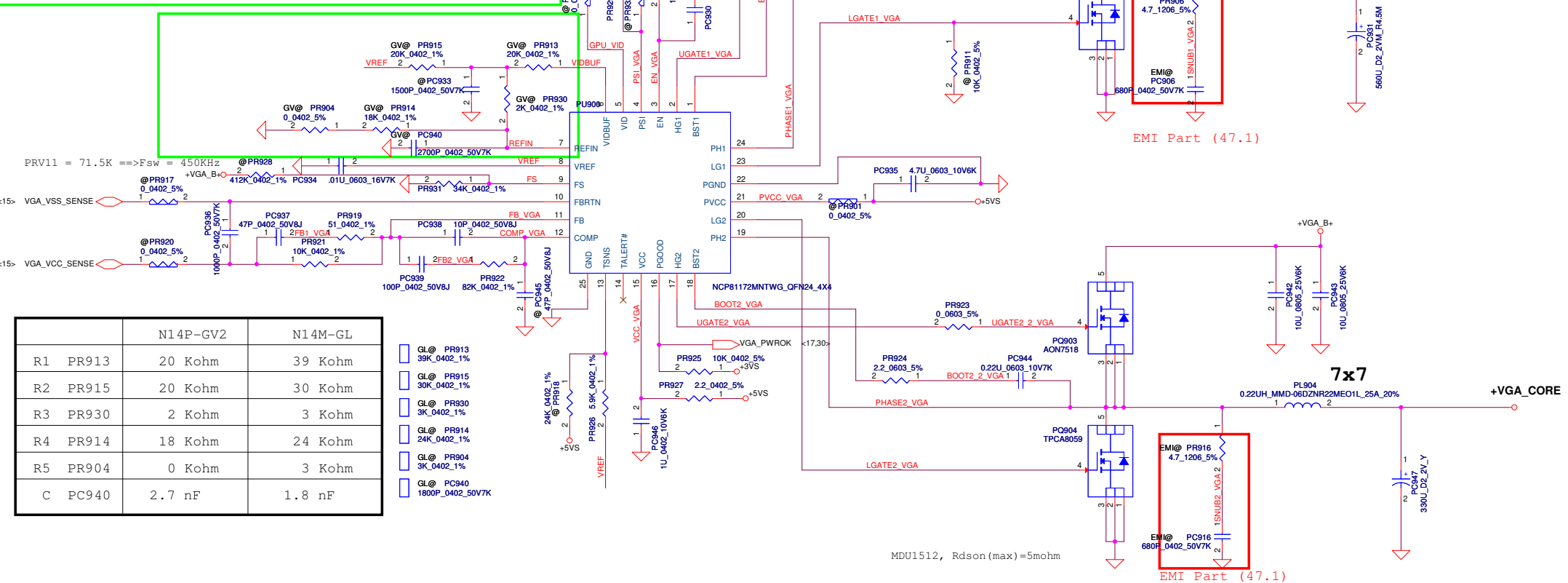
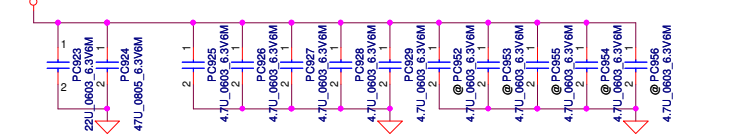


Chief River ULV	330uF*9m	22uF	10uF	2.2uF	1uF	470uF	560uF
CPU	2	14		16			
GFX_CORE		6	6		11	1	
1.05V_VCCP			10		26		1

+VGA_CORE Under VGA Core **GB4-128 package**



+VGA_CORE Near VGA Core



	N14P-GV2	N14M-GL
R1 PR913	20 Kohm	39 Kohm
R2 PR915	20 Kohm	30 Kohm
R3 PR930	2 Kohm	3 Kohm
R4 PR914	18 Kohm	24 Kohm
R5 PR904	0 Kohm	3 Kohm
C PC940	2.7 nF	1.8 nF

- ☐ GL@ PR913
39K_0402_1%
- ☐ GL@ PR915
30K_0402_1%
- ☐ GL@ PR930
3K_0402_1%
- ☐ GL@ PR914
24K_0402_1%
- ☐ GL@ PR904
3K_0402_1%
- ☐ GL@ PC940
1800P_0402_50V7K

MDU1512, Rdson (max)=5mohm

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Issued Date	2012/09/24	Deciphered Date	2013/09/24	Title +VGA COREP		
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				Custom	VFKTA	0.3
Date:				Sheet	53	of 56

Item	Reason for change	PG#	Modify List	Date	Phase
1		45			
2		45			
3					
4		46			
5		47			
6		49			
7		49			
8		49			
9		49			
10		48			
11		47			
12		47			
13		44			
14		44			
15		46			
16		47			
17		49			
18		49			
19		45			
20		45			
21		47			
22		47			
23		45			
24		46			
25		47			
26		48			
27		43			

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				Size	Document Number	Rev
				Custom	VFKTA	0.3
Date:				Thursday, January 17, 2013	Sheet 54 of 56	

HW PIR (Product Improve Record)

VFKTA LA-9861P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	11/13	39	Add CA39 (SE102104K00)	BOM structure change
2.	11/13	39	Reserve RA31,RA38	EMI request
3.	11/13	41	Change RB36 from 2.2k to 0 ohm and CB50 to @	Design change
4.	11/13	15	Update VGA strap pin all page	Design change
5.	11/21	42	Remove NFC function	Design change
6.	11/21	42	Update CPU config&PN	Design change
7.	11/26	23	change BOM structure C238,C239,C240,C241,C242,C243 to CRT@EMI@	EMI request
8.	11/26	22	Add D92 for LID_SW#_D to isolate the +3VL power rail from LID_SW#	Design change
9.	11/26	24	Add @ to JHDMI	Design change
10.	11/26	37	Change JCARD.10 to SDWP# and JCARD.11 to SDCD.	Design change
		37	Add QW1, RW3, RW4 for normal close type connector.	
11.	11/26	40	Update HDMI power circuit	Design change
12.	11/26	40	Change JSPK from 8 pin to 6 pin (SP02000WS00)	Design change
13.	11/26	40	Remove SPK_DET1 and change SPK_DET0 net name to SPK_DET	Design change
14.	11/26	39	Change RA50 to 269@	Design change
15.	11/26	40	Reverse JSPK to keep same layout routing on MB	Design change
16.	11/27	30	Remove GPIO71 and change SPK_DET1 to SPK_DET	Design change
17.	11/29	30	Add GPIO22 as VRAM_DR_SR# and add RH203, RH205 for BOM control <DIS>	For dual&single rank common bios
18.	11/30	30	Change RH202, RH203 BOM structure to GVDR@ and GVSR@	For dual&single rank common bios
19.	11/30	42	Change H7 to 4P0, Add H19 (3P2N), Change H17, H18 to PTH	ME request
20.	11/30	25	Change UH3 from socket to IC	Design change
21.	11/30	09	Change CC53 to 47U 0805 (SE000000PL00)& add CC50 (SE000000PL00)	For 1206 MLCC Crack issue
		09	Change CC44 to 47U 0805 (SE000000PL00)& add CC40 (SE000000PL00)	
		12	Change CD31 to 47U 0805 (SE000000PL00)	
		38	Change CR10&CR12 to 47U 0805 (SE000000PL00)	
22.	11/30	07	Change RC73 to 0 ohm (do not use short pad on this location)	For debug
23.	11/30	17	Change RV53 pull high to +3VS	Design change
24.	11/30	15	Change RV24 to 4.99K	Strap pin change
25.	11/30	22	Delete D92 and change the netname to BKOFF#	Avoid LCD_INV leak to Touch/B
26.	11/30	23	Add R62 & R63 for CRT undershoot issue	For CRT undershoot issue
27.	11/30	25	Chane UH4, RH269, RH271 to @, change RH267 from shortpad to 0-ohm @.	Design change
28.	11/30	08	Add CC17~CC19 for ESD request	ESD request
29.	11/30	29,41	Move PLT_RST# ESD capacitor (CH104) to EC side (CB13) and mount 0.1uF	ESD request
30.	11/30	05	Change CC63 from @ESD@ to ESD@	ESD request
31.	11/30	41	Change PM_SLP_S4# from pin127 to pin84.	For ENE common code
32.	11/30	41	Change USB_EN#0 from pin84 to pin23.	For ENE common code
33.	11/30	41	Change FB_CLAMP from pin23 to pin127.	For ENE common code
34.	11/30	17	CV57 and CV60 change to 0.01U.	For sequence
35.	11/30	17	RV47 change to 180K.	For sequence
36.	12/03	38	Update USB circuit	For S&C MAX4640 and MAX4641 co-lay circuit
37.	12/04	42	Change H19 to NPTH	Design change
38.	12/04	17	Change QV2 footprint to NC7ST32P5X_SC70-5	For non-A51 part change
39.	12/04	04	Add S&C SMBus address in the table	Design change

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				Custom		0.3
				Date	Thursday, January 17, 2013	Sheet 55 of 56

HW PIR (Product Improve Record)

QCLA4 LA-8861P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
40.	12/04	41	Add short-pad (RB5) on pin127.	Design change
41.	12/04	13	Reverse DV1, Change DV1, QV8 to OPT@,	
		13	Change FB_CLAMP_MON from pull down to pull high +3VS_DGPU	
42.	12/04	17	Change UV2 PN to SA007320300	Design change
		17	Change UV2, CV58 to OPT@ and change RV50 to @	
43.	12/04	43	Add R5546 put high PCH_PWR_EN to +3VL	Design change
45.	12/05	41	Add CHG_PWR_GATE# pull high 3VL and add RB11 10K.	Design change
46.	12/05	38	S&C IC Pin1 was connected to the EC(GPIO49) Pin82.	Design change

VFKTA LA-9861P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	12/24	17	Change RV43 to 270K	For GC6 timing requirements
2.	12/24	17	Change RV53 to 10K	For GC6 timing requirements
3.	12/24	17	Change RV54 to 33K	For GC6 timing requirements
4.	12/24	17	Change RV50to N14MGL@	N14M-GL doesn't support GC6
5.	12/24	17	Change UV2to N14PGV2@	N14M-GL doesn't support GC6
6.	12/24	17	Change CV58 to @	Cost reduction
7.	12/24	13	Change QV8to N14PGV2@	N14M-GL doesn't support GC6
8.	12/24	13	Change DV1 P/N to SCS000002G00	BOM reduction
9.	01/09	41	Change CB31 to 100P P/NSE071101J80	Design Change
10.	01/09	7, 9, 25	Change QC3, QC7, QC8, QH1 to SB000000PF00	SB501380020 X1 code
11.	01/15	22	Reserve R267&R266 0 ohm	For EMI cost down
12.	01/15	41	Reserve CB50 1U	Common design
13.	01/15	13	GPIO12 be connected to EC_GPXIOA01(remove EC_DRAMRST_CNTRL_PCH&RC3)	For GPS
14.	01/16	42	Modify JTP pin define	For DFB highlight
15.	01/16	22	Add C17 100P on LED_PWM	For EMI request
16.	01/17	39/42	Add RB12, RB37, connect EC_MUTE_INT from codec to EC	For boot bobo issue
17.	01/17	5/30/42	Reserve CC1, CH1, CB17, CB18, CC35 100P	For ESD

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				Custom		0.3
				Date:	Thursday, January 17, 2013	Sheet 56 of 56

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